

EA53\_BM  
Schematics Document

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Cover Page

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Sheet

1

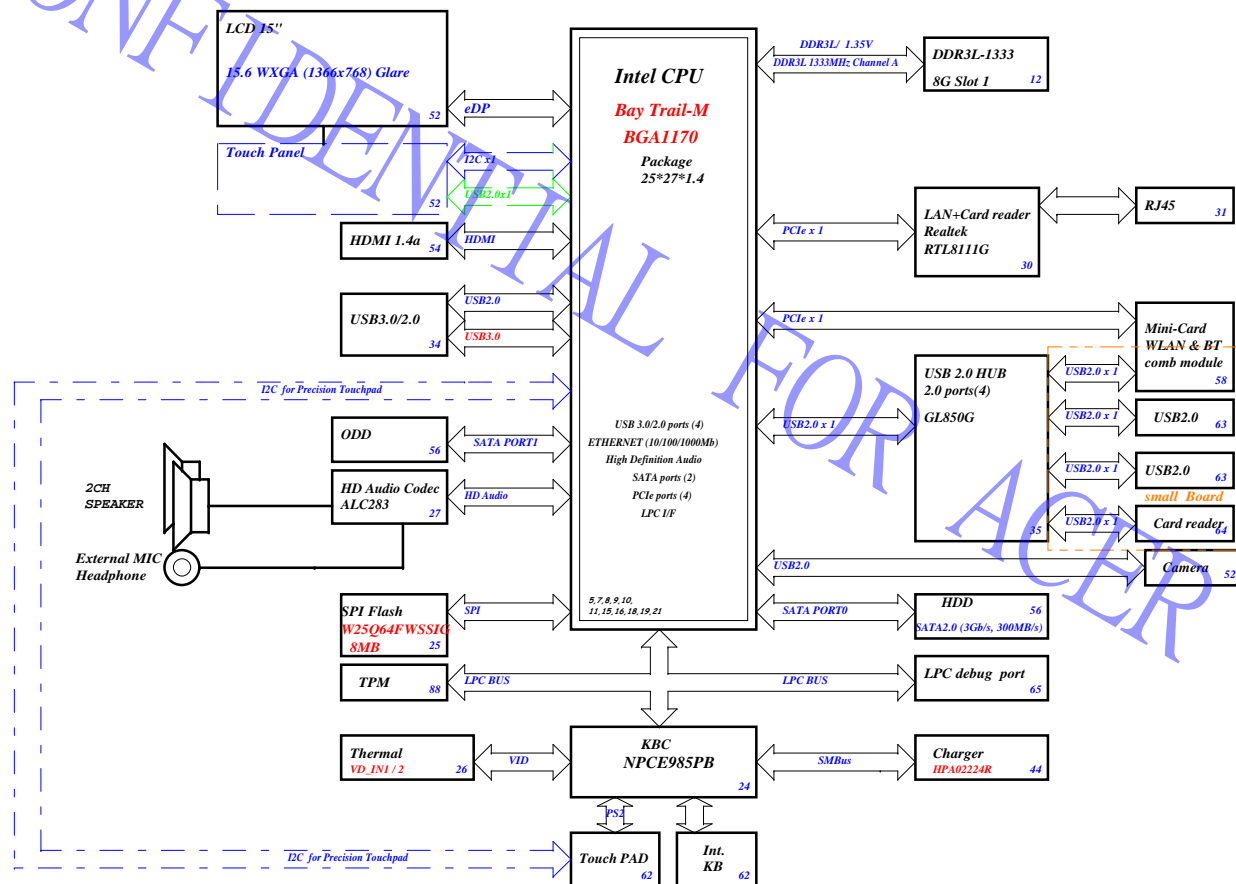
of

102

# EA53-BM Board Block Diagram

Project code : 4PD037010001  
PCB P/N : 14222  
Revision : -1

CHARGER	
PAK22	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575B	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC	
RT6575B	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
TPS51716	50
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
SYSTEM DC/DC	
TPS51716	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM LDO	
RT9198	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930	51
INPUTS	OUTPUTS
3D3V_S5	1D0V_S5



## PCB LAYER

L1:Top L4:signal  
L2:VCC L5:GND  
L3:signal L6:Bottom

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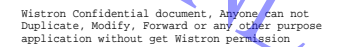
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CPU1I 9 OF 13		
BAY TRAIL-M/D SOC		
A11	VSS1	VSS36
A15	VSS2	VSS37
A19	VSS3	VSS38
A23	VSS4	VSS39
A27	VSS5	VSS40
A31	VSS6	VSS41
A35	VSS7	VSS42
A39	VSS8	VSS43
A43	VSS9	VSS44
A47	VSS10	VSS45
AA1	VSS11	VSS46
AA16	VSS12	VSS47
AA19	VSS13	VSS48
AA21	VSS14	VSS49
AA3	VSS15	VSS50
AA32	VSS16	VSS51
AA35	VSS17	VSS52
AA39	VSS18	VSS53
AA53	VSS19	VSS54
AB10	VSS20	VSS55
AB4	VSS21	VSS56
AB41	VSS22	VSS57
AB45	VSS23	VSS58
AB47	VSS24	VSS59
AB48	VSS25	VSS60
AB50	VSS26	VSS61
AB51	VSS27	VSS62
AB6	VSS28	VSS63
AC16	VSS29	VSS64
AC18	VSS30	VSS65
AC19	VSS31	VSS66
AC21	VSS32	VSS67
AC25	VSS33	VSS68
AC33	VSS34	VSS69
AC35	VSS35	VSS70
BAY-TRAIL-GP		GP

CPU1J 10 OF 13		
BAY TRAIL-M/D SOC		
AG38	VSS71	VSS106
AH4	VSS72	VSS107
AH41	VSS73	VSS108
AH45	VSS74	VSS109
AH7	VSS75	VSS110
AH9	VSS76	VSS111
AJ1	VSS77	VSS112
AJ16	VSS78	VSS113
AJ21	VSS79	VSS114
AJ25	VSS80	VSS115
AJ27	VSS81	VSS116
AJ29	VSS82	VSS117
AJ3	VSS83	VSS118
AJ30	VSS84	VSS119
AJ32	VSS85	VSS120
AJ33	VSS86	VSS121
AJ35	VSS87	VSS122
AJ38	VSS88	VSS123
AJ53	VSS89	VSS124
AK10	VSS90	VSS125
AK14	VSS91	VSS126
AK16	VSS92	VSS127
AK33	VSS93	VSS128
AK41	VSS94	VSS129
AK44	VSS95	VSS130
AM12	VSS96	VSS131
AM19	VSS97	VSS132
AM24	VSS98	VSS133
AM25	VSS99	VSS134
AM29	VSS100	VSS135
AM33	VSS101	VSS136
AM35	VSS102	VSS137
AM36	VSS103	VSS138
AM40	VSS104	VSS139
M28	VSS105	VSS140
BAY-TRAIL-GP		GP

CPU1K 11 OF 13		
BAY TRAIL-M/D SOC		
AT24	VSS141	VSS176
AT27	VSS142	VSS177
AT30	VSS143	VSS178
AT35	VSS144	VSS179
AT38	VSS145	VSS180
AT4	VSS146	VSS181
AT47	VSS147	VSS182
AT52	VSS148	VSS183
AU1	VSS149	VSS184
AU24	VSS150	VSS185
AU3	VSS151	VSS186
AU30	VSS152	VSS187
AU38	VSS153	VSS188
AU51	VSS154	VSS189
AV12	VSS155	VSS190
AV13	VSS156	VSS191
AV14	VSS157	VSS192
AV18	VSS158	VSS193
AV19	VSS159	VSS194
AV24	VSS160	VSS195
AV27	VSS161	VSS196
AV30	VSS162	VSS197
AV35	VSS163	VSS198
AV38	VSS164	VSS199
AV47	VSS165	VSS200
AV51	VSS166	VSS201
AV7	VSS167	VSS202
AW13	VSS168	VSS203
AW19	VSS169	VSS204
AW27	VSS170	VSS205
AW3	VSS171	VSS206
AW35	VSS172	VSS207
AY10	VSS173	VSS208
AY22	VSS174	VSS209
AY32	VSS175	VSS210
BAY-TRAIL-GP		GP

CPU1L 12 OF 13		
BAY TRAIL-M/D SOC		
BF30	VSS211	VSS246
BF36	VSS212	VSS247
BF4	VSS213	VSS248
BG31	VSS214	VSS249
BG34	VSS215	VSS250
BG39	VSS216	VSS251
BG42	VSS217	VSS252
BG45	VSS218	VSS253
BG49	VSS219	VSS254
BJ11	VSS220	VSS255
BJ15	VSS221	VSS256
BJ19	VSS222	VSS257
BJ23	VSS223	VSS258
BJ27	VSS224	VSS259
BJ31	VSS225	VSS260
BJ35	VSS226	VSS261
BJ39	VSS227	VSS262
BJ43	VSS228	VSS263
BJ47	VSS229	VSS264
BJ7	VSS230	VSS265
C14	VSS231	VSS266
C31	VSS232	VSS267
C34	VSS233	VSS268
C39	VSS234	VSS269
C42	VSS235	VSS270
C45	VSS236	VSS271
C49	VSS237	VSS272
D12	VSS238	VSS273
D16	VSS239	VSS274
D24	VSS240	VSS275
D30	VSS241	VSS276
D36	VSS242	VSS277
D38	VSS243	VSS278
E19	VSS244	VSS279
E35	VSS245	VSS280
BAY-TRAIL-GP		GP

CPU1M 13 OF 13		
BAY TRAIL-M/D SOC		
K9	VSS281	VSS316
L13	VSS282	VSS317
L19	VSS283	VSS318
L35	VSS284	VSS319
M19	VSS285	VSS320
M26	VSS286	VSS321
M27	VSS287	VSS322
M34	VSS288	VSS323
M35	VSS289	VSS324
M38	VSS290	VSS325
M47	VSS291	VSS326
M51	VSS292	VSS327
N1	VSS293	VSS328
N16	VSS294	VSS329
N38	VSS295	VSS330
N51	VSS296	VSS331
P13	VSS297	VSS332
P16	VSS298	VSS333
P19	VSS299	VSS334
P20	VSS300	VSS335
P24	VSS301	VSS336
P32	VSS302	VSS337
P35	VSS303	VSS338
P38	VSS304	VSS339
P4	VSS305	VSS340
P47	VSS306	VSS341
P52	VSS307	VSS342
P9	VSS308	VSS343
T30	VSS309	VSS344
U1	VSS310	VSS345
U11	VSS311	VSS346
U12	VSS312	VSS347
U14	VSS313	VSS348
U21	VSS314	VSS349
VSS315	VSS350	VSS350
BAY-TRAIL-GP		GP

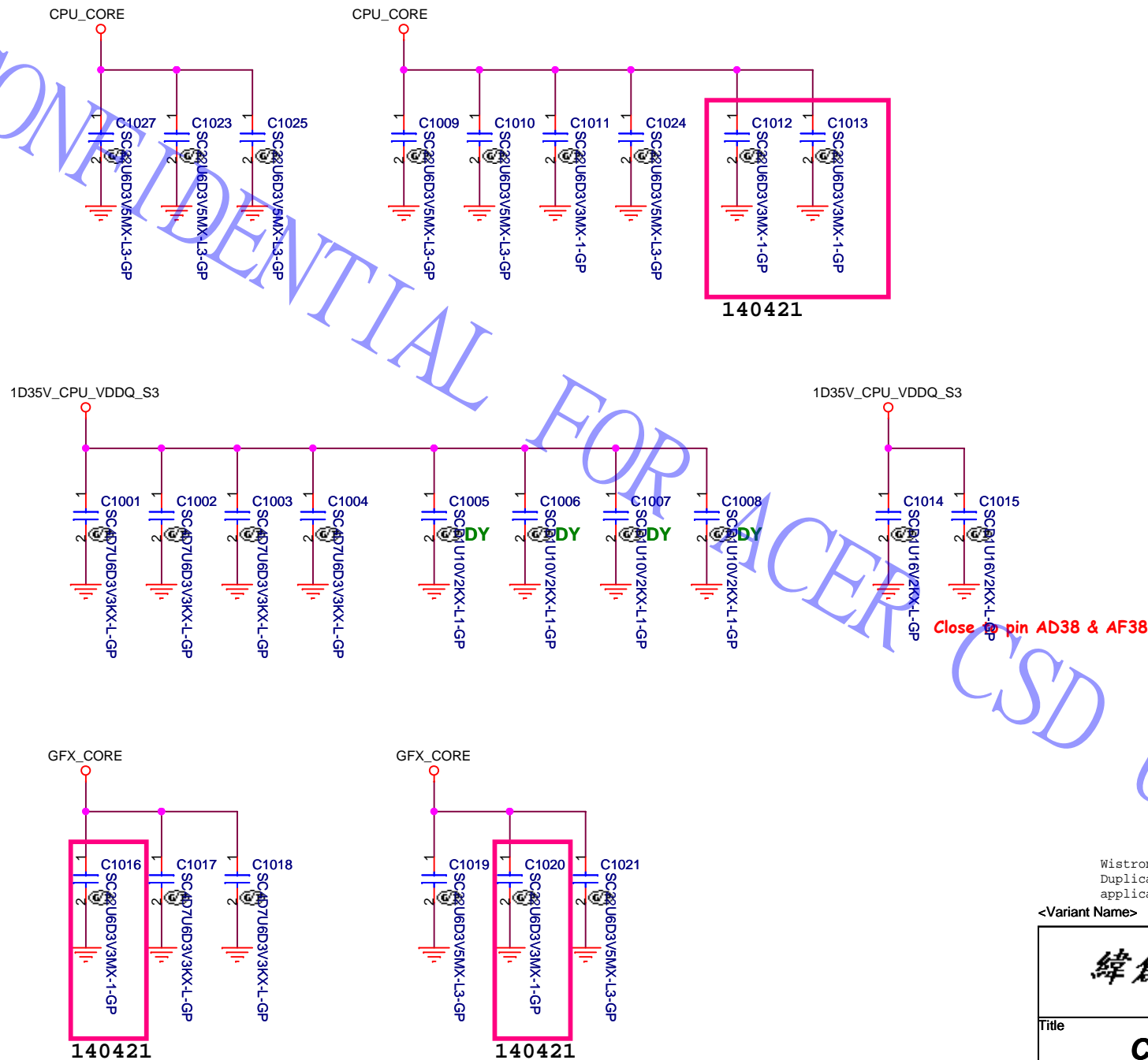
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**CPU (Power CAP1)**

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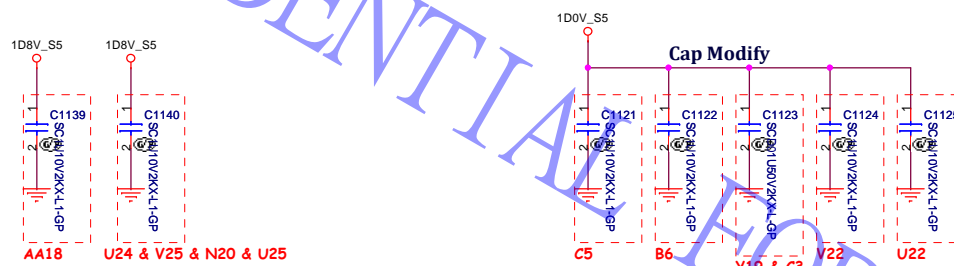
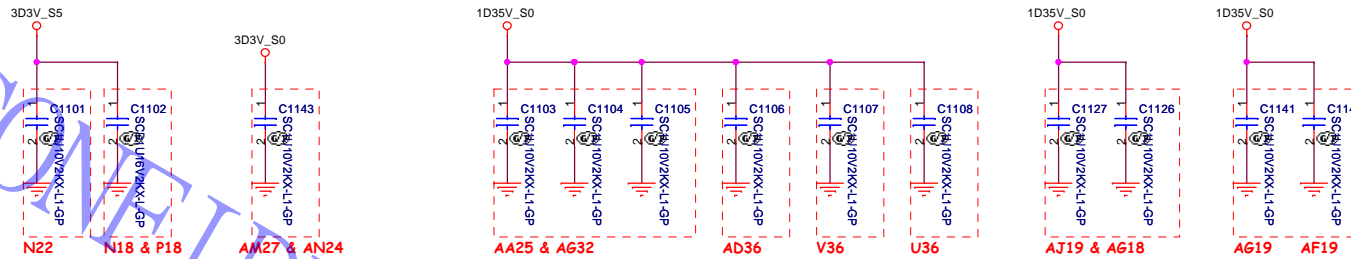
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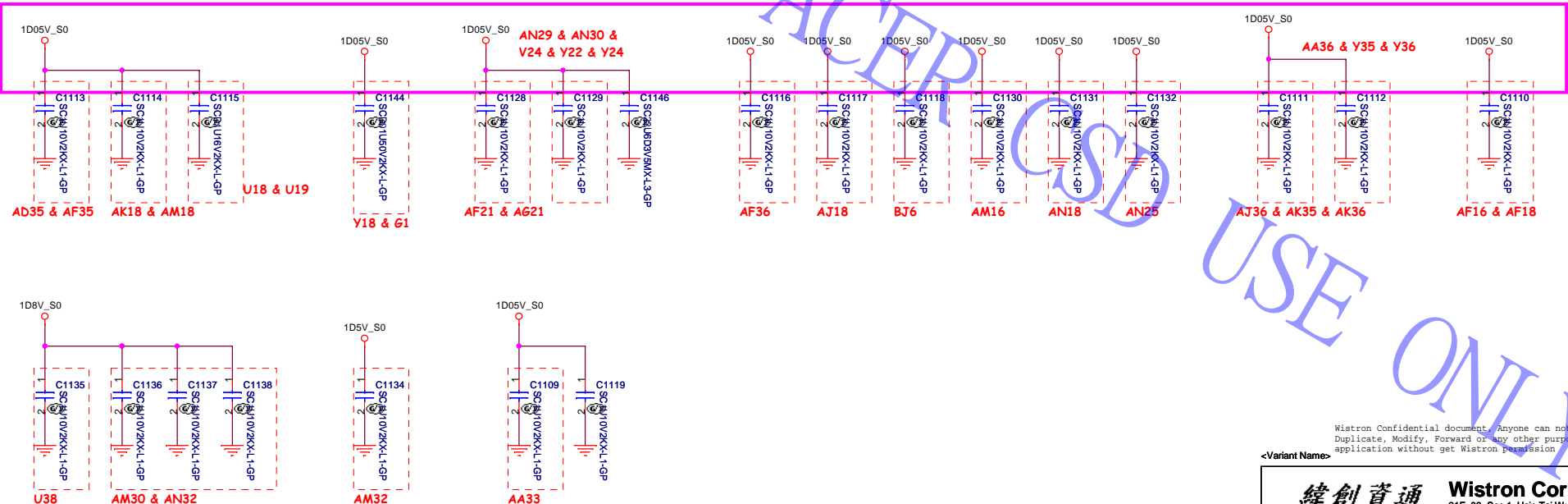
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# Cap Modify



## 1D0V change to 1D05V



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0726\_SA

3D3V\_50

1DDEV\_50

R1212  
2K2R2J-1-GP

C1201

Q1201  
DMNSL08K-7-GP

SMB\_CLK\_DIMM

SMB\_CLK\_CPU 16

3D3V\_50

1DDEV\_50

R1213  
2K2R2J-1-GP

C1202

Q1202  
DMNSL08K-7-GP

SMB\_DATA\_DIMM

SMB\_DATA\_CPU 16

$$V_{GS(th)} = 1V$$

For Intel Recommend Close to DIMM(Bay Trail)

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SSID = MEMORY

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Size A2	Document Number EA53-BM Rev -1
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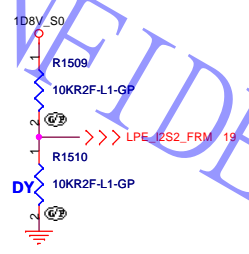
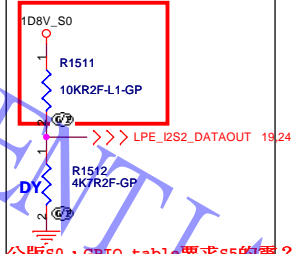
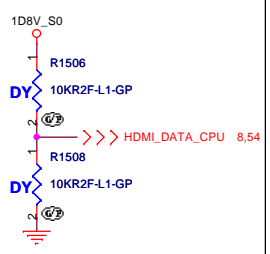
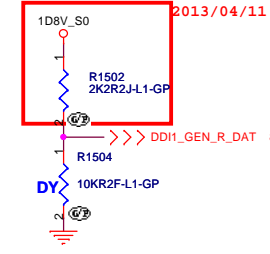
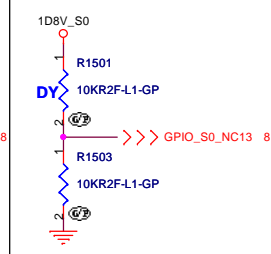
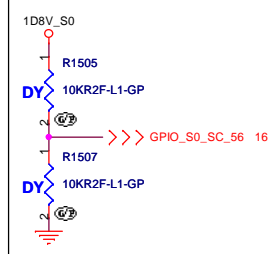
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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

## 2.25 Hardware Straps

All straps are sampled on the rising edge of PMC\_CORE\_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

## 30.2 LPE\_I2S2\_DATAOUT / GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

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Pair	Device
0	USB3.0 Port 0(USB2.0)
1	Touch Panel ((Debug port))
2	USB HUB
3	Camera



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SSID = PCH

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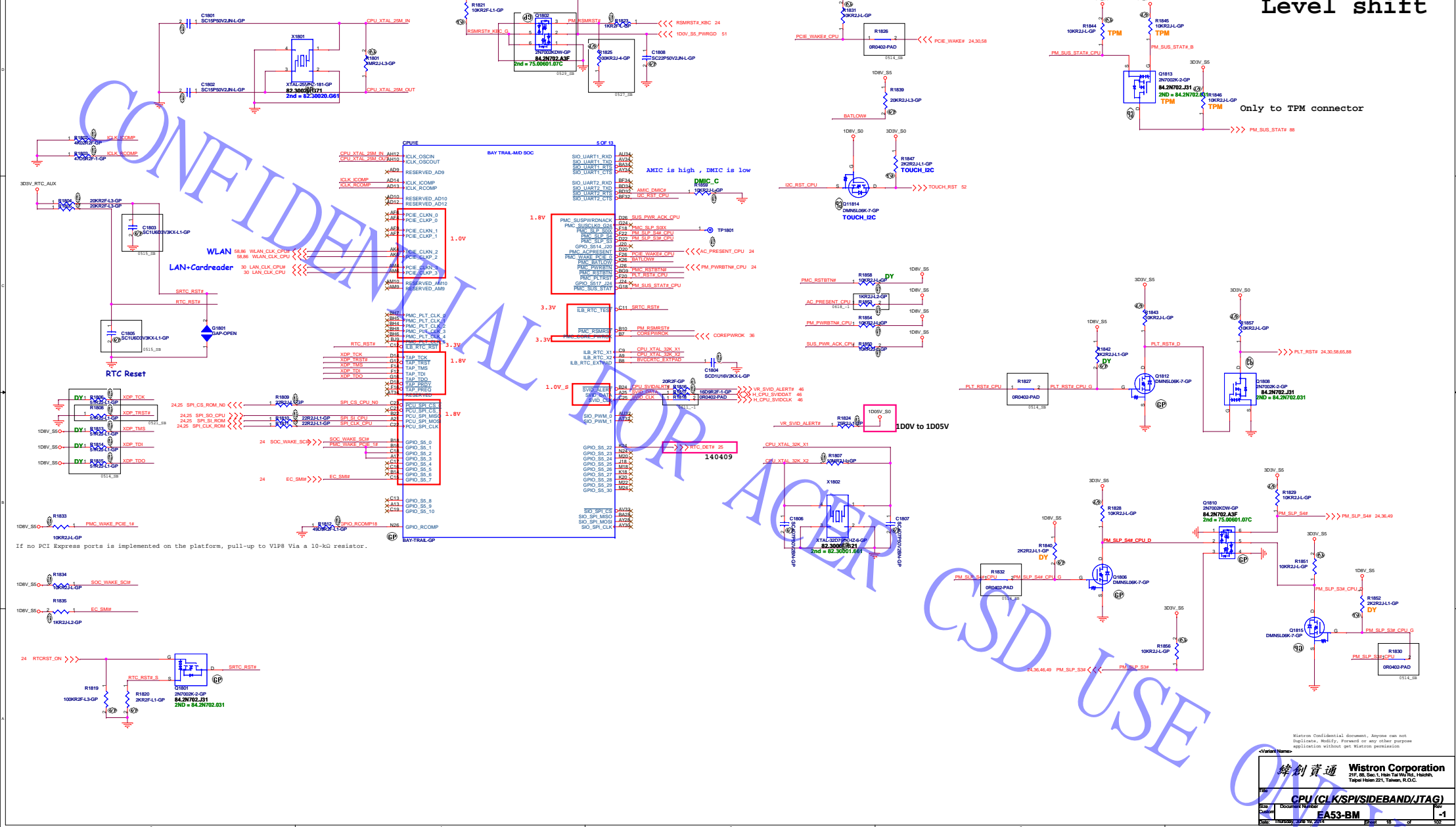
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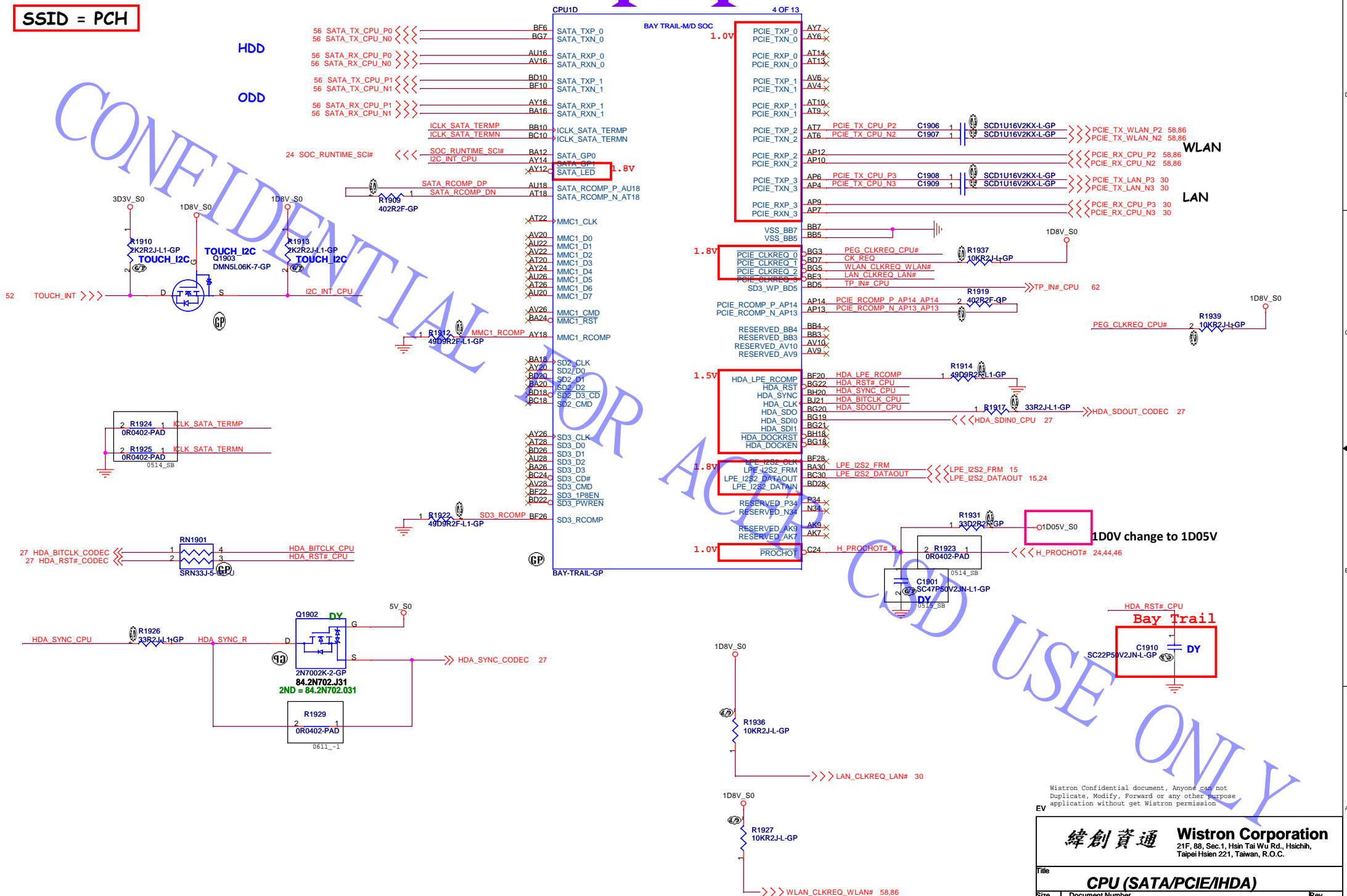
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ODD



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<b>CPU (VSS)</b>			
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PCB_Vin_A0	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	≈ 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	≈ 2.616 V < 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	≈ 2.363 V < 2.616 V
-I	100.0 K	47.0 K	2.245 V	2.2592	2.2305	≈ 2.123 V < 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	≈ 1.934 V < 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	≈ 1.758 V < 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	≈ 1.504 V < 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	≈ 1.281 V < 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	≈ 1.126 V < 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	≈ 0.924 V < 1.126 V

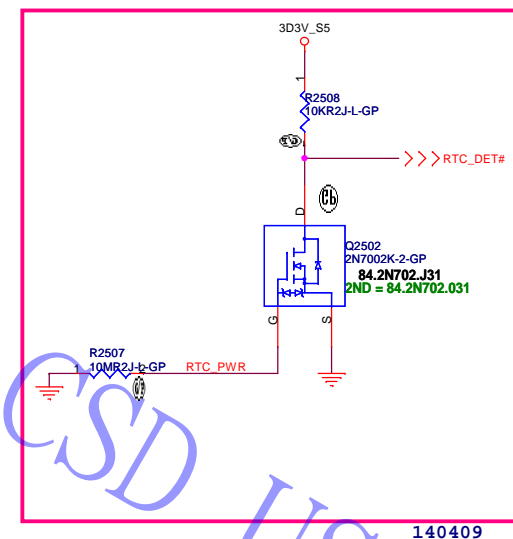
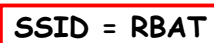
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Title		<b>KBC NPCE985</b>	
Size	Document Number	Rev	
Custom	<b>EA53-BM</b>		-1
Date	Thursday, June 19, 2014	Sheet	24 of 102



SPI FLASH ROM (8M byte) IC PCH



Title			
<b>Flash(KBC+PCH)/RTC</b>			
Size	Document Number	Rev	
A3	<b>EA53-BM</b>	<b>-1</b>	
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5V\_S0



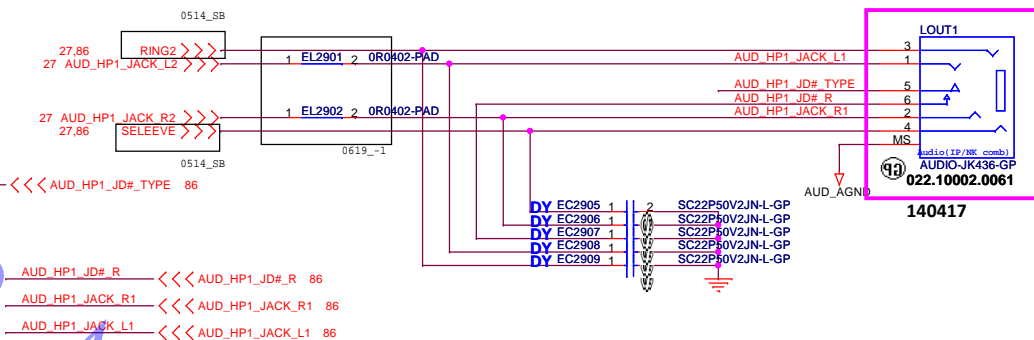
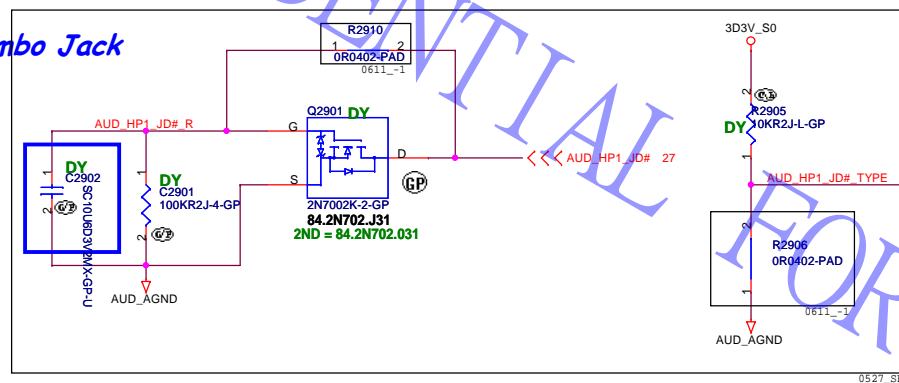
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# Blanking

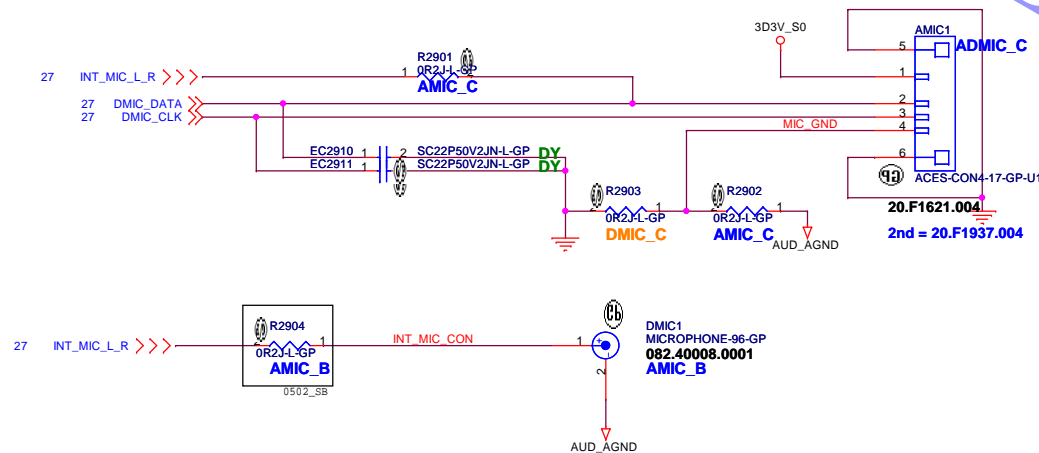
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**DMIC AMIC**

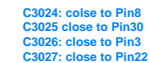


AMIC on board: mount DMIC1, R2904, DY AMIC1, R2901, R2902, R2903, EC2910, EC2911  
AMIC for cable: mount AMIC1, R2901, R2902, DY R2903, EC2910, EC2911, DMIC1, R2904  
DMIC for cable: mount AMIC1, R2903, DY R2901, R2902, EC2910, EC2911, DMIC1, R2904

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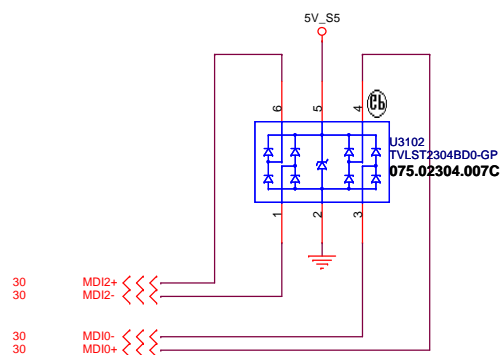
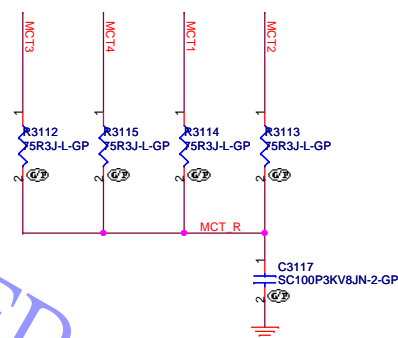
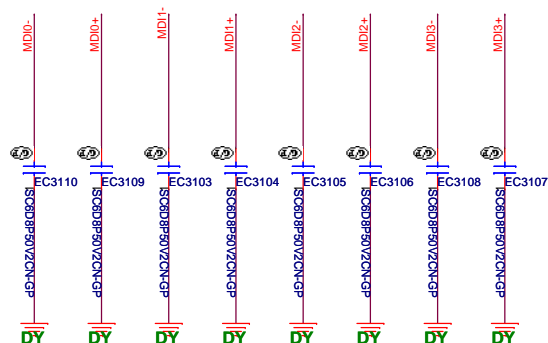
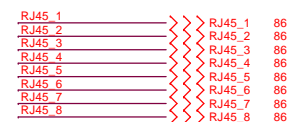
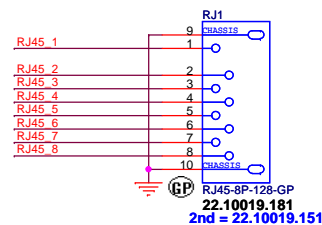
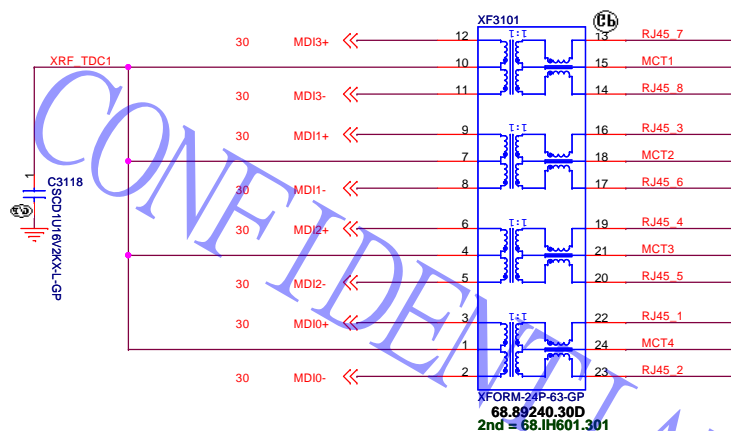
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Title			
<b>Audio Jack</b>			
Size	Document Number	Rev	
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SSID = LAN

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Title

**RTS5170(CARD READER)**

Size  
A4

Document Number

**EA53-BM**

Rev  
**-1**

Date: Wednesday, June 04, 2014

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SSID = SDIO

SD//MS Card Reader

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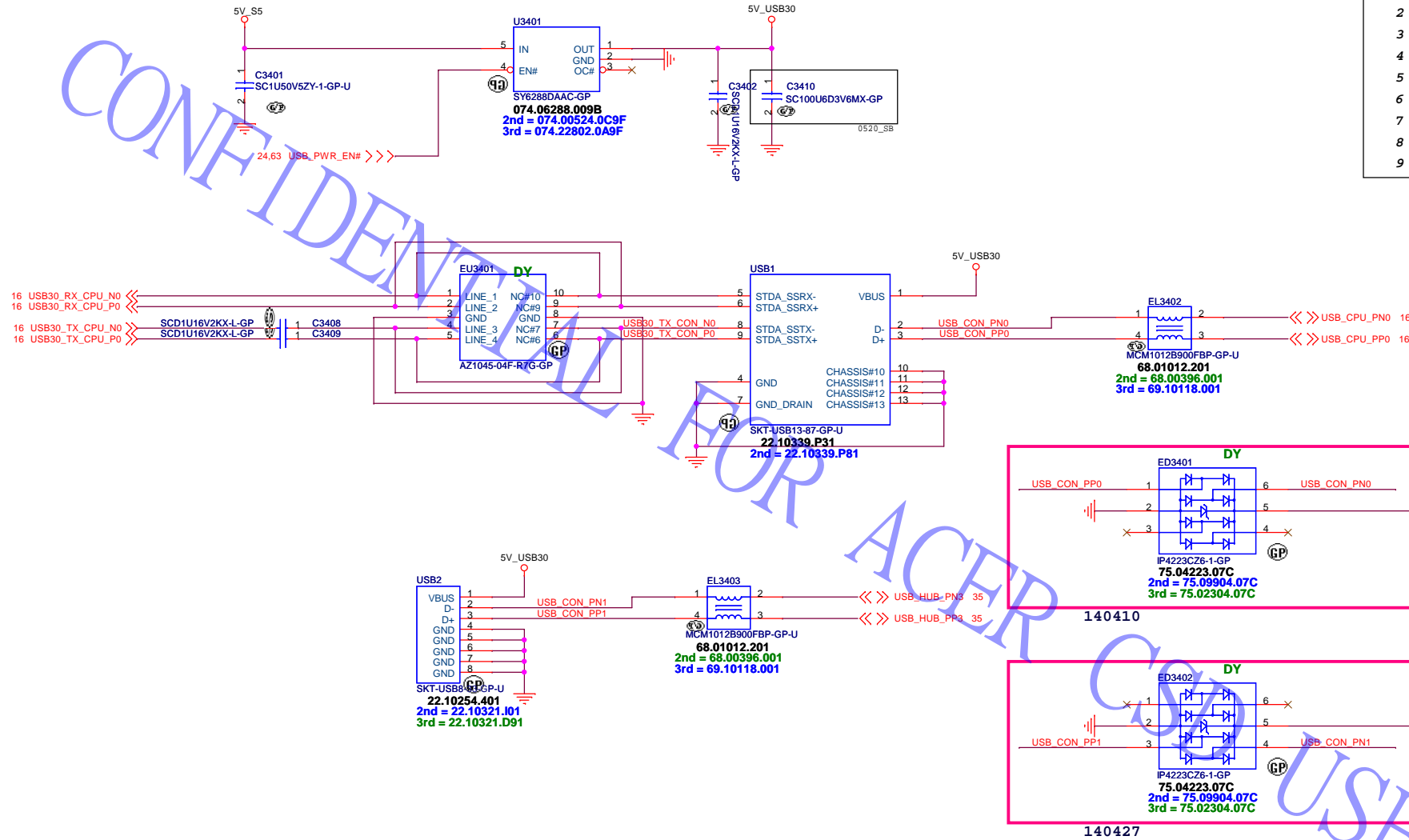
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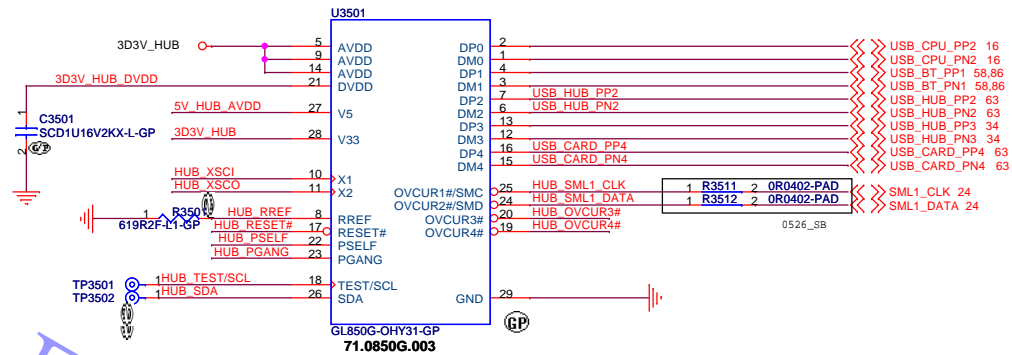
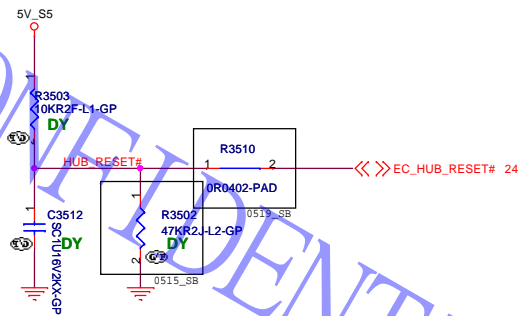
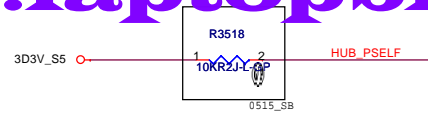
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Title			
CARD Reader CONN			
Size	Document Number		Rev
Custom	EA53-BM		-1
Date:	Wednesday, June 04, 2014		Sheet 33 of 102

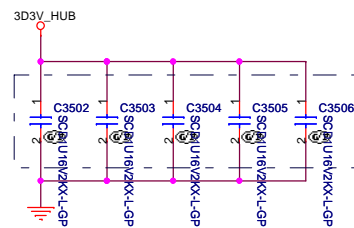
Low Active 2A



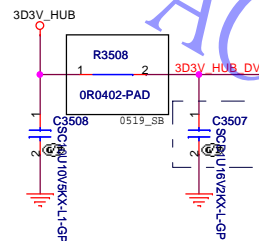
USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



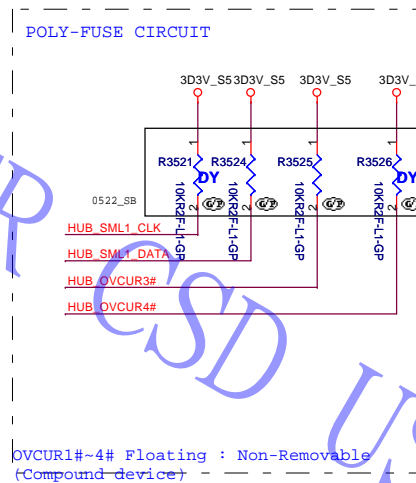
CPU  
WLAN(Bluetooth)  
USB 2.0(SMBD)  
USB 2.0  
Card reader



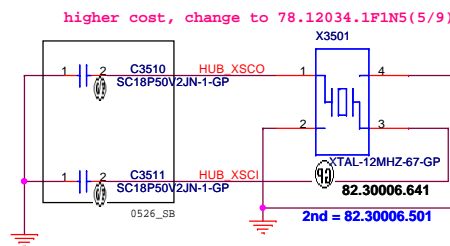
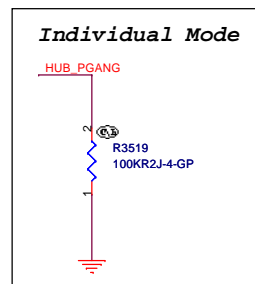
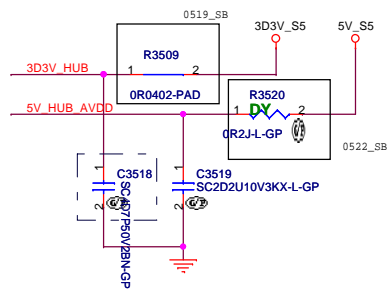
As close to GL850G-32



EC1 close to PIN28



OVCUR1#~4# Floating : Non-Removable (Compound device)



higher cost, change to 78.12034.1F1N5(5/9)

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<p>Title: <b>USB HUB</b></p>	
<p>Size: Custom</p>	<p>Document Number: <b>EA53-BM</b></p>
<p>Date: Thursday, June 19, 2014</p>	<p>Sheet 35 of 102</p>
<p>Rev: <b>-1</b></p>	

Power Sequence

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

ALL\_SYS\_PWRGD

13/8/22  
To EC

From EC

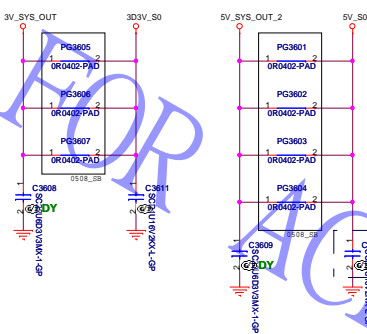
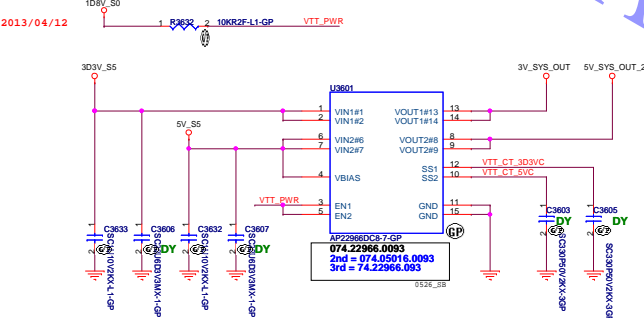
Delay 104ms with ALL\_SYS\_PWRGD

COREPWROK

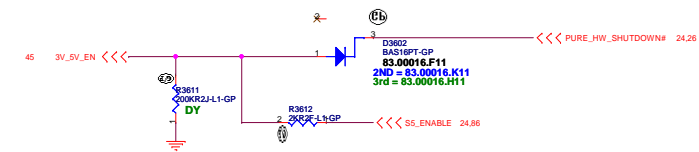
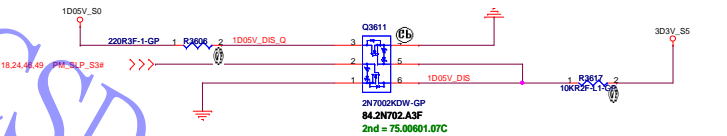
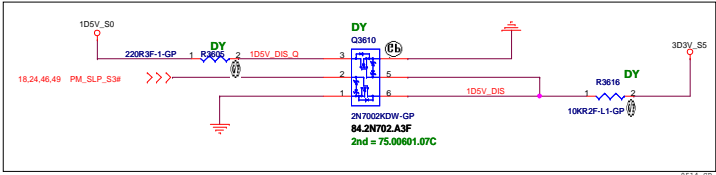
ANNIE Run Power

13/9/18

2013/04/09

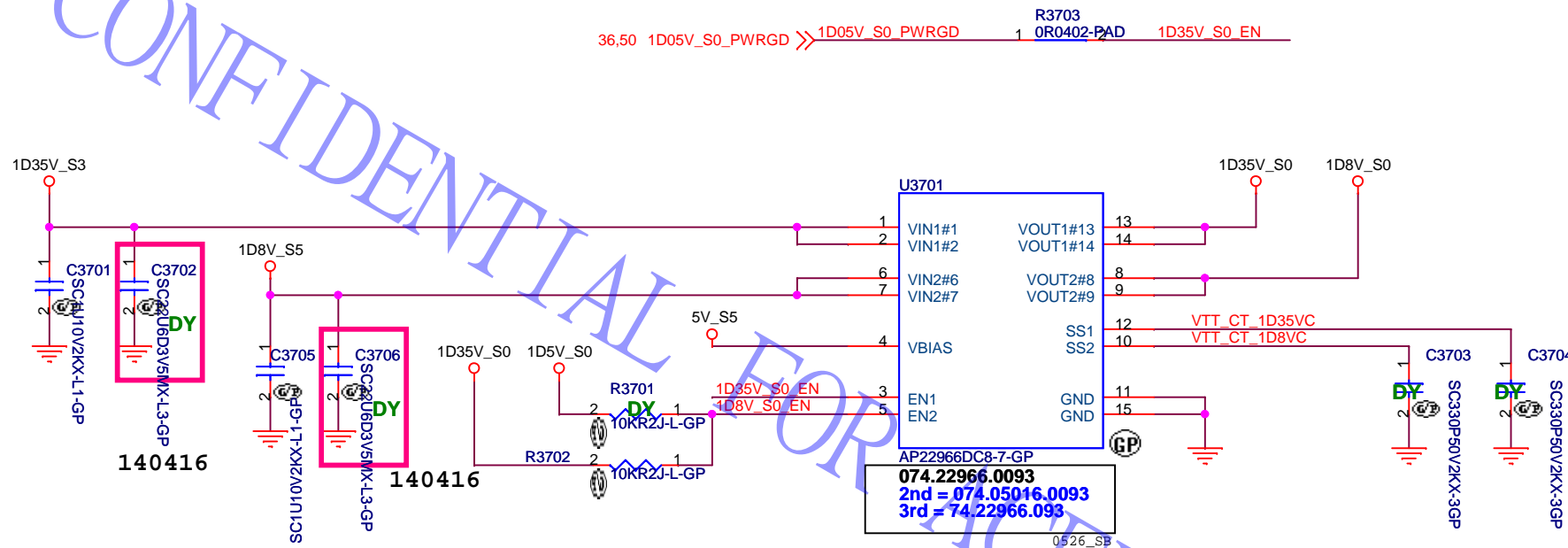


Discharge circuit



1D35V\_S0

1D8V\_S0



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Title

ADAPTER OCP / S3 reduction

Size  
A4

Document Number

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Rev  
-1

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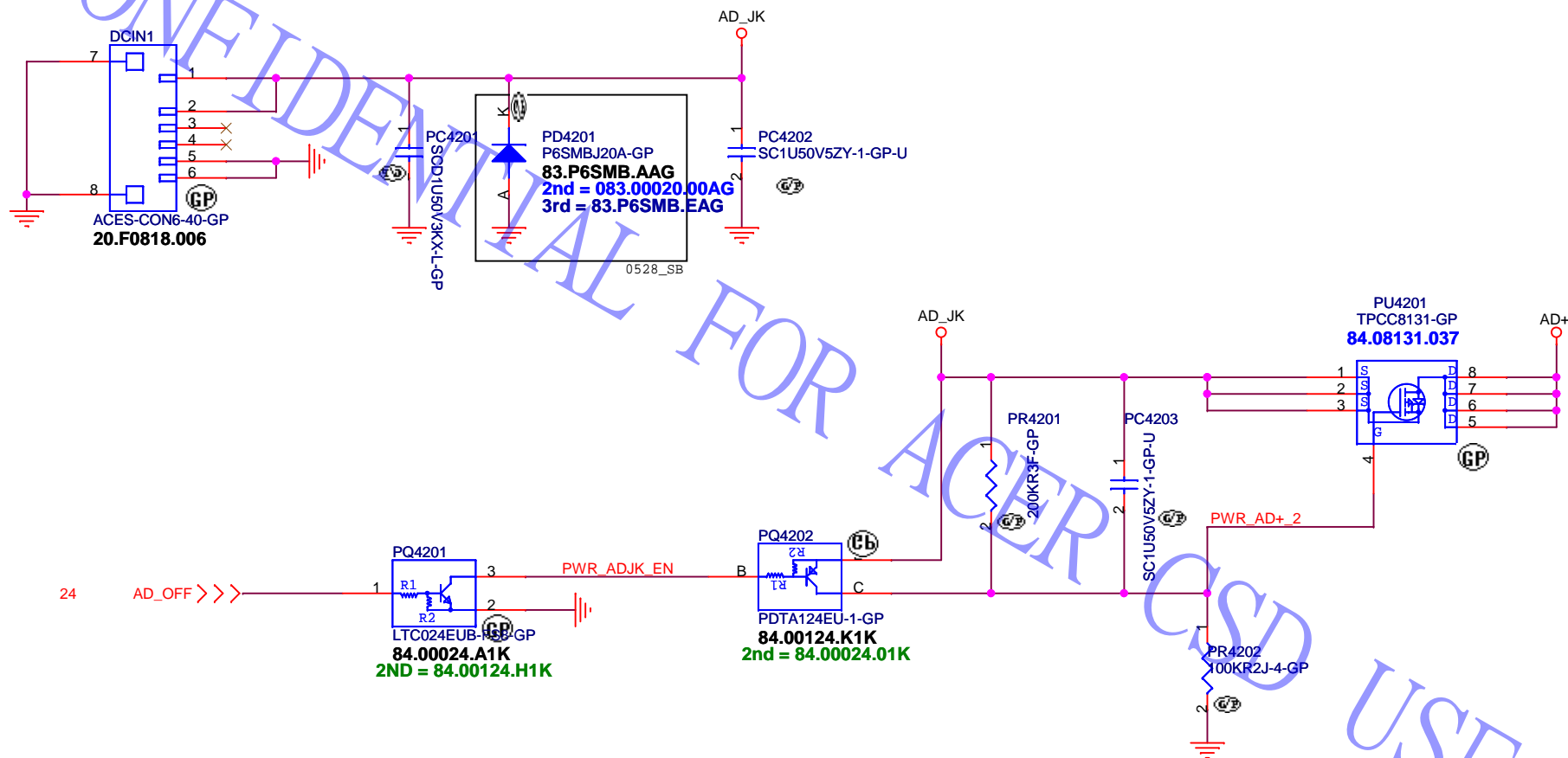
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## Adaptor in to generate DCBATOUT



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Title

DCIN JACK

Size  
A4

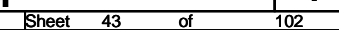
Document Number

EA53-BM

Rev  
-1

Date: Thursday, June 19, 2014

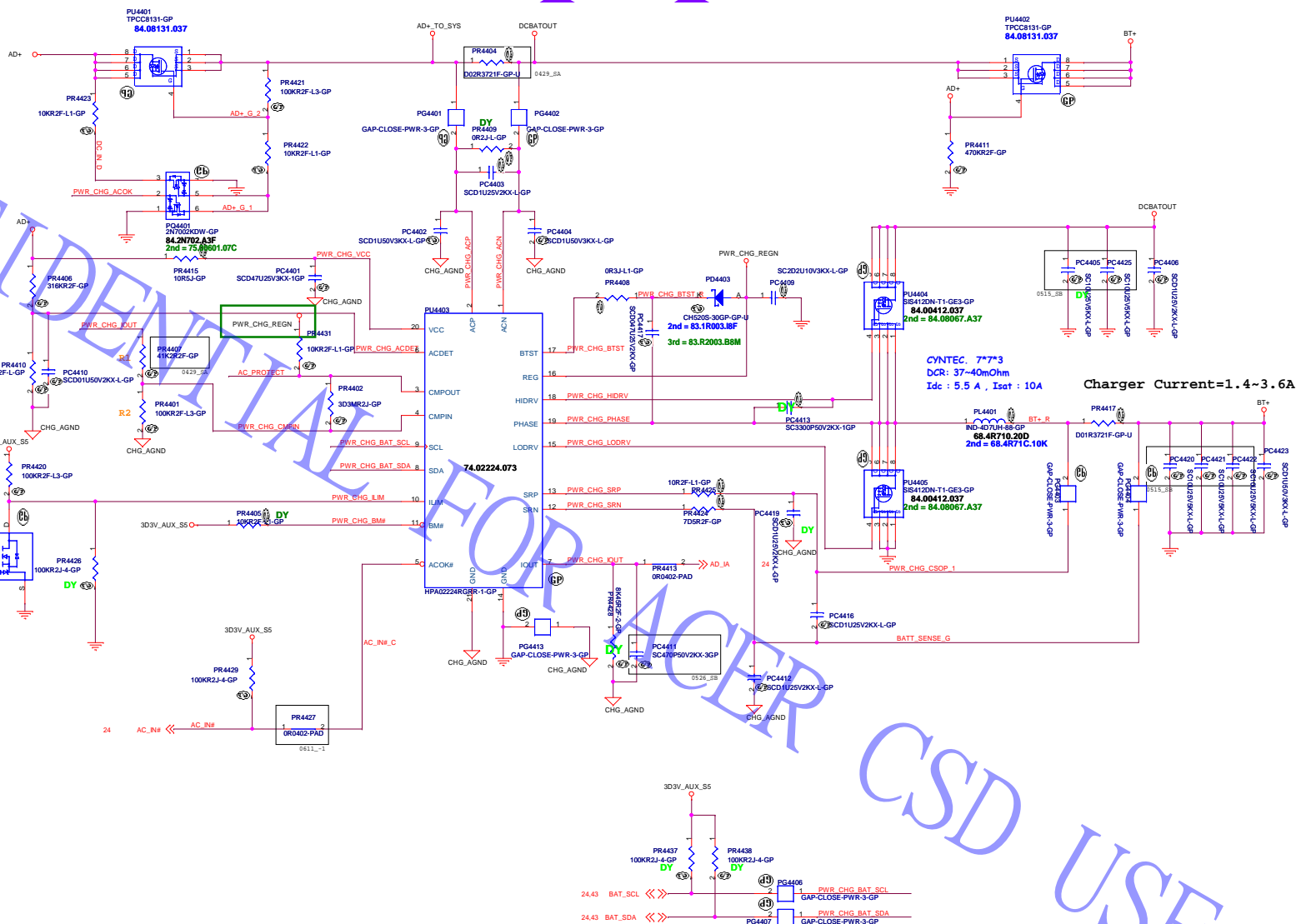
Sheet 42 of 102



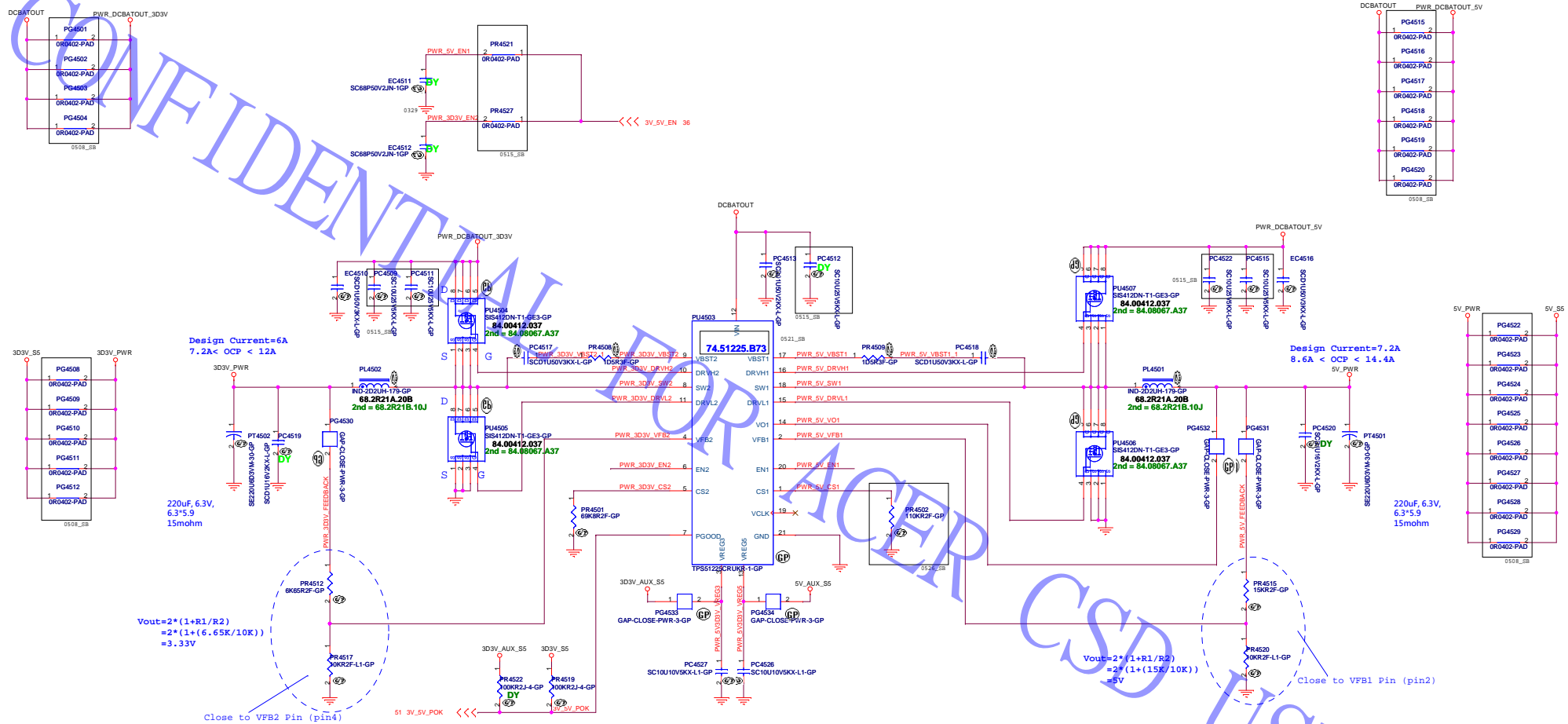
**www.laptopblue.vn**

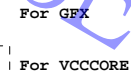
AD+ total power	R1	R2
40w	41.2K	100K

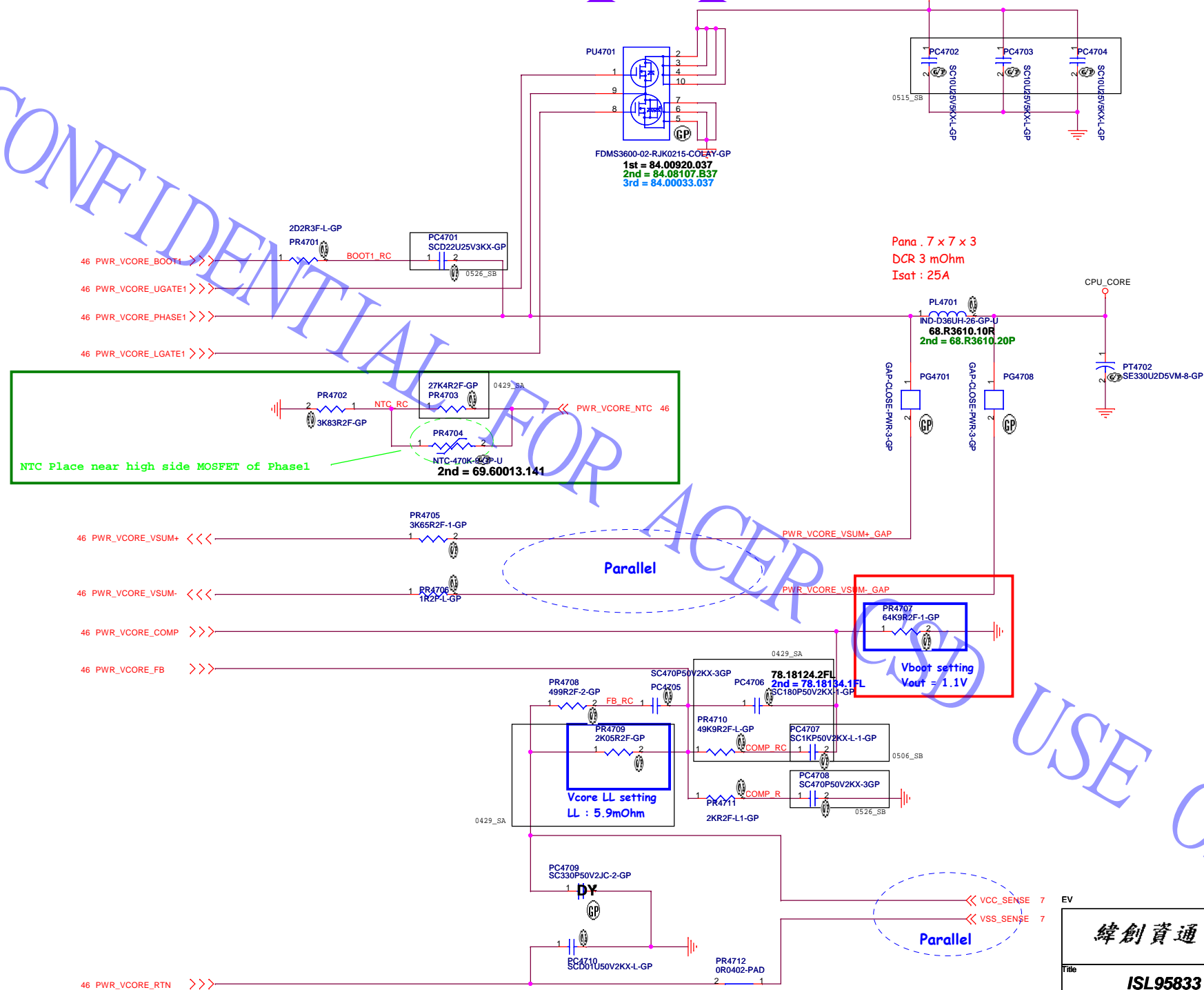
2014/04/29

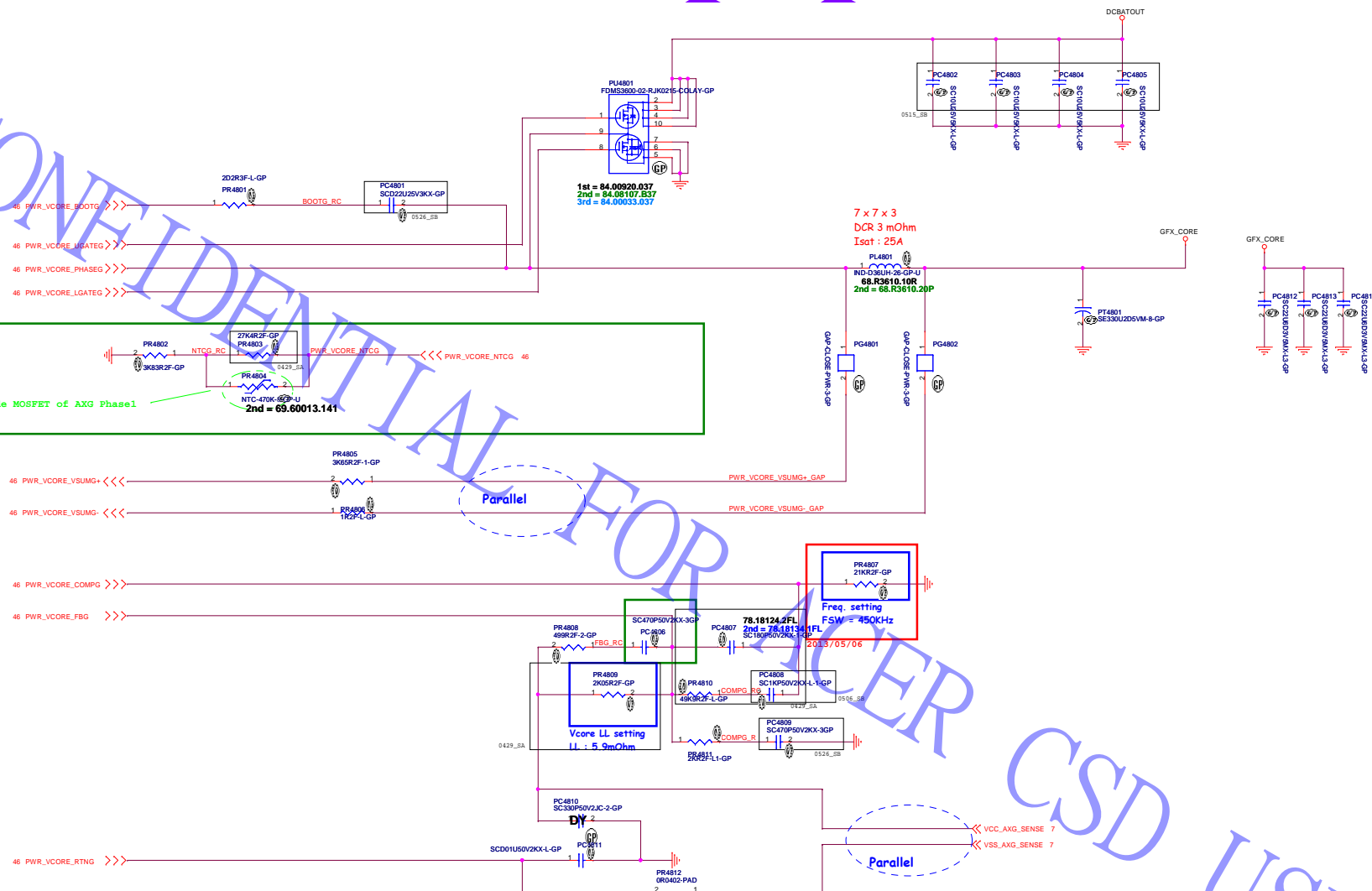


Charger Current=1.4~3.6A





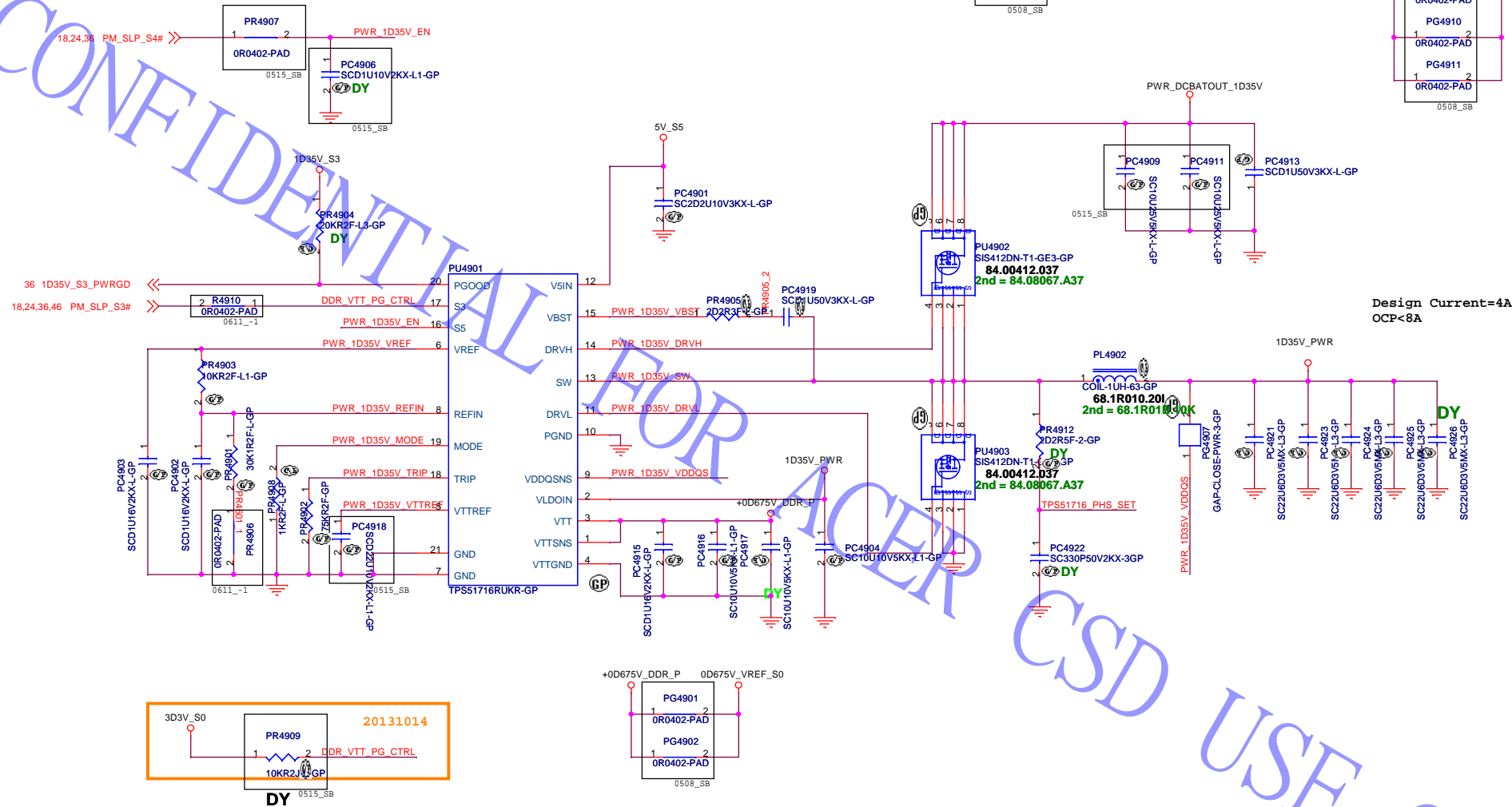






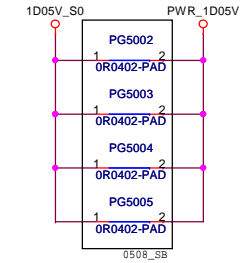
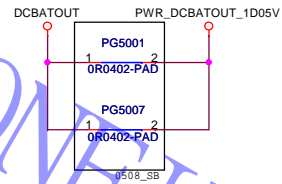
SSID = PWR.Plane.Regulator 1p35v6p675v

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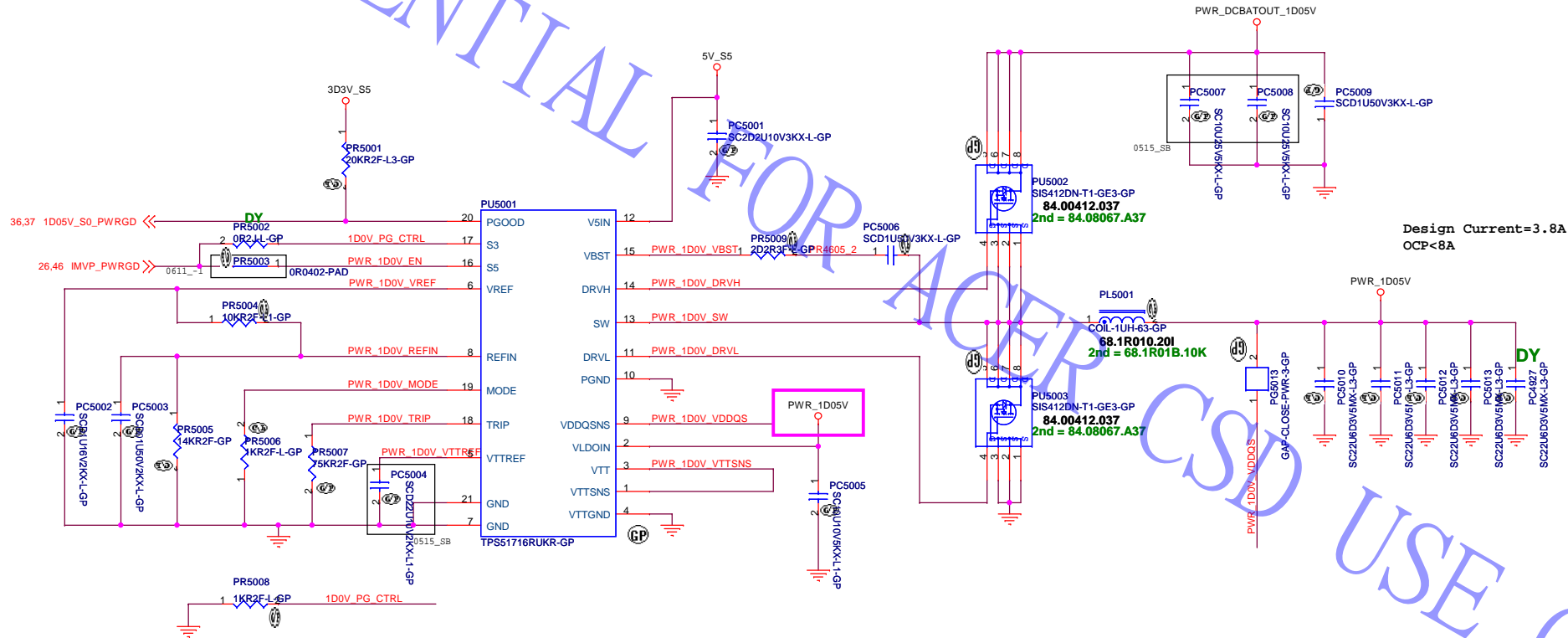


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



## TPS51716 for 1D05V\_S0



Design Current=3.8A  
OCP<8A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

### MODE

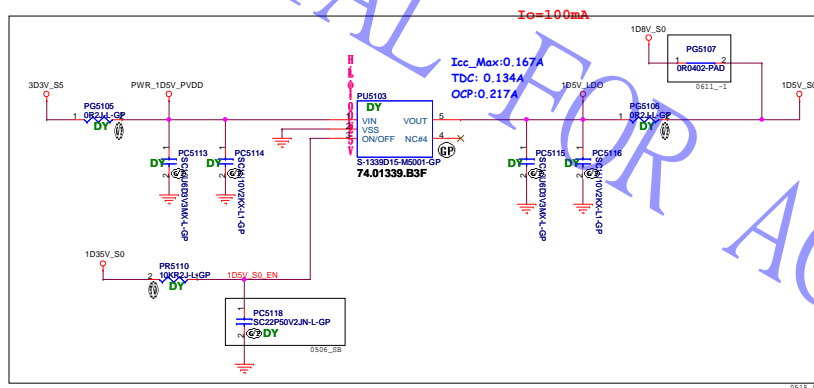
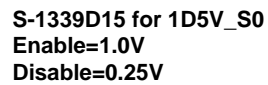
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	Non-tracking Discharge
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	Tracking Discharge

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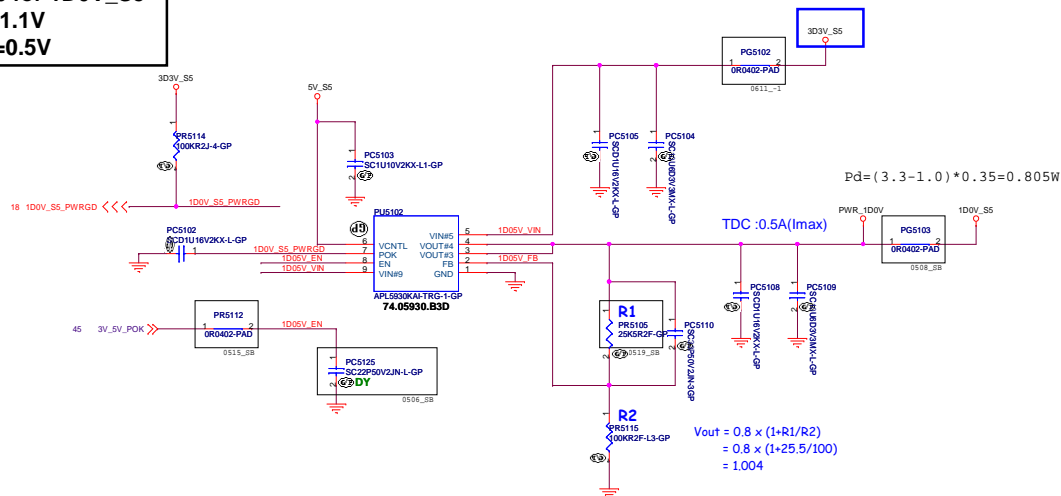
EV

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Title <b>DC to DC 1D05V(TPS51716)</b>	
Size A3	Document Number <b>E453-BM</b>
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**Disable=0.6V**



**APL5930 for 1D0V\_S5**  
**Enable=1.1V**  
**Disable=0.5V**



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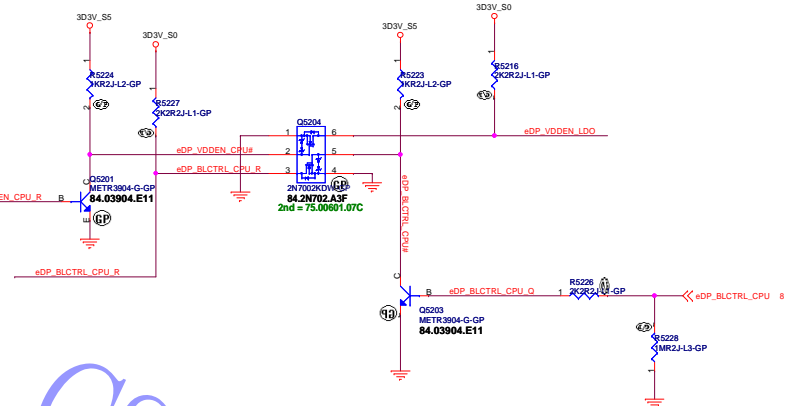
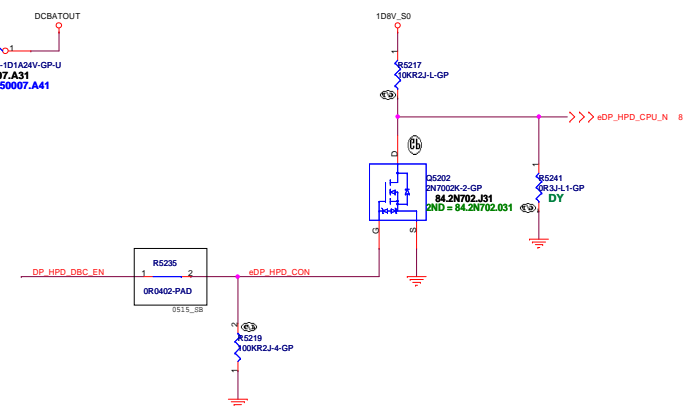
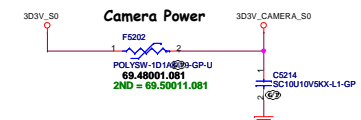
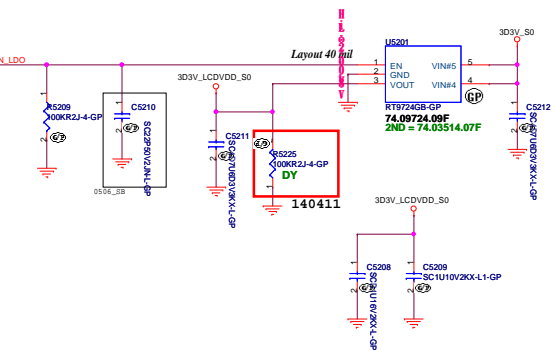
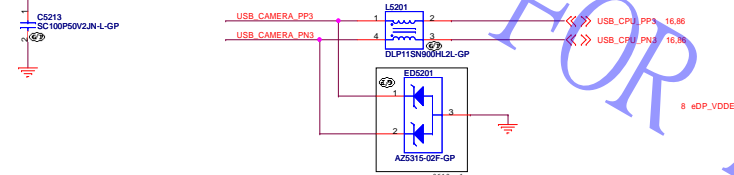
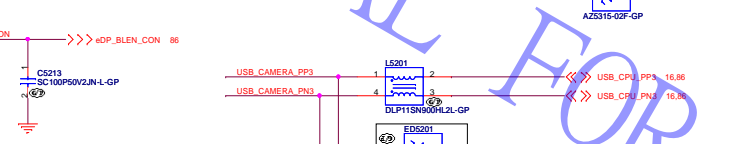
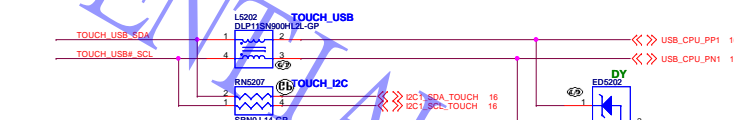
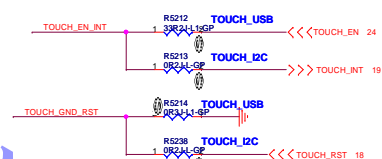
Pinout diagram of the Star Line Camera Module. The diagram shows the connections for the LVDS1 interface and other signals. The pins are numbered 1 through 36. The connections are as follows:

- Pin 1: LVDS1
- Pin 2: DP AUXP LVDS DATA
- Pin 3: DP ALXN LVDS CLK
- Pin 4: DP TXP0 LVDSA D0 R
- Pin 5: DP TXP0 LVDSA D0 RB
- Pin 6: DP TXP1 LVDSA D1 R
- Pin 7: DP TXP1 LVDSA D1 RB
- Pin 8: TOUCH IRB6\_SCL
- Pin 9: TOUCH IRB6\_SDA
- Pin 10: TOUCH IRB6\_SCK
- Pin 11: TOUCH IRB6\_EN
- Pin 12: TOUCH IRB6\_RST
- Pin 13: TOUCH IRB6\_INT
- Pin 14: TOUCH IRB6\_EN
- Pin 15: TOUCH IRB6\_RST
- Pin 16: TOUCH IRB6\_INT
- Pin 17: TOUCH IRB6\_EN
- Pin 18: TOUCH IRB6\_RST
- Pin 19: TOUCH IRB6\_INT
- Pin 20: TOUCH IRB6\_EN
- Pin 21: TOUCH IRB6\_RST
- Pin 22: TOUCH IRB6\_INT
- Pin 23: TOUCH IRB6\_EN
- Pin 24: TOUCH IRB6\_RST
- Pin 25: TOUCH IRB6\_INT
- Pin 26: TOUCH IRB6\_EN
- Pin 27: TOUCH IRB6\_RST
- Pin 28: TOUCH IRB6\_INT
- Pin 29: TOUCH IRB6\_EN
- Pin 30: TOUCH IRB6\_RST
- Pin 31: TOUCH IRB6\_INT
- Pin 32: TOUCH IRB6\_EN
- Pin 33: TOUCH IRB6\_RST
- Pin 34: TOUCH IRB6\_INT
- Pin 35: TOUCH IRB6\_EN
- Pin 36: TOUCH IRB6\_RST

Additional connections shown in the diagram include:

- Pin 1: R5220
- Pin 2: R5220
- Pin 3: R5220
- Pin 4: R5220
- Pin 5: R5220
- Pin 6: R5220
- Pin 7: R5220
- Pin 8: R5220
- Pin 9: R5220
- Pin 10: R5220
- Pin 11: R5220
- Pin 12: R5220
- Pin 13: R5220
- Pin 14: R5220
- Pin 15: R5220
- Pin 16: R5220
- Pin 17: R5220
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- Pin 20: R5220
- Pin 21: R5220
- Pin 22: R5220
- Pin 23: R5220
- Pin 24: R5220
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- Pin 26: R5220
- Pin 27: R5220
- Pin 28: R5220
- Pin 29: R5220
- Pin 30: R5220
- Pin 31: R5220
- Pin 32: R5220
- Pin 33: R5220
- Pin 34: R5220
- Pin 35: R5220
- Pin 36: R5220

The diagram also shows the connection for the STAR CON3A (DP) and the STAR CON3A (DP) to the STAR CON3A (DP) and the STAR CON3A (DP) to the STAR CON3A (DP).



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Title

CRT Connector

Size

A3

Document Number

EA53-BM

Date

Wednesday, June 04, 2014

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of

102

Rev

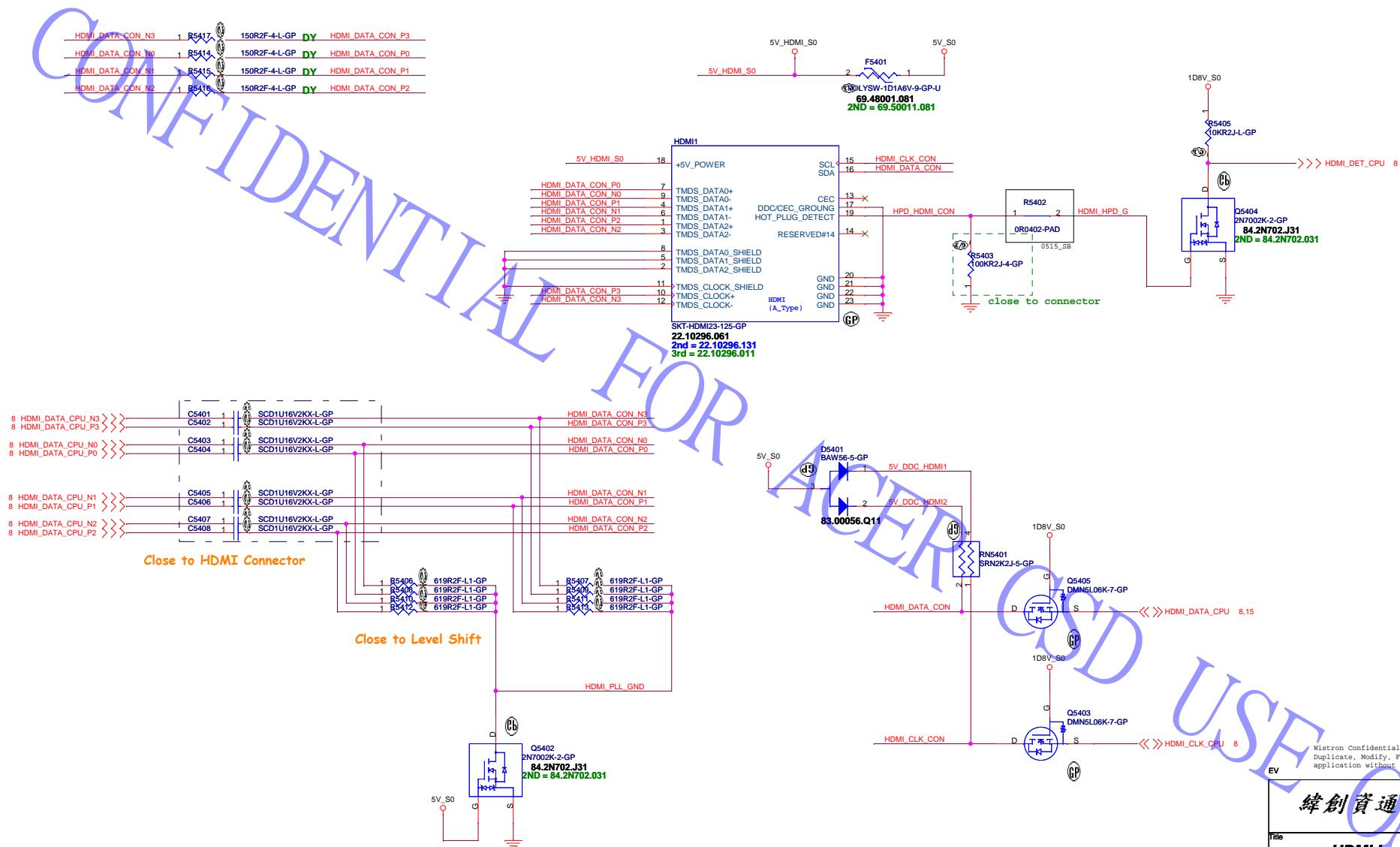
-1

SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

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HDMI Level Shifter/Connector			
Size	Document Number	Rev	-1
Custom	EA53-BM		
Date	Thursday, June 19, 2014	Sheet	54 of 102

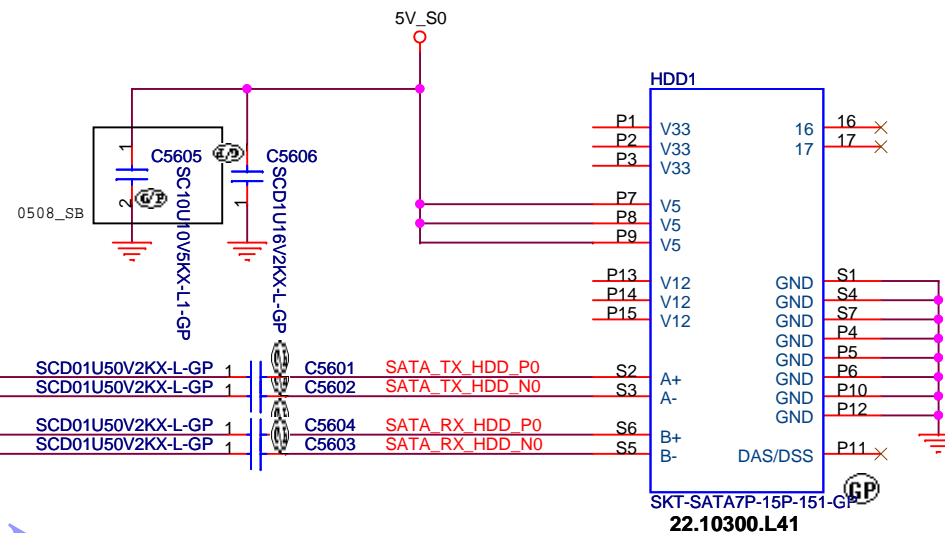
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Reserved					
Size	Document Number				Rev
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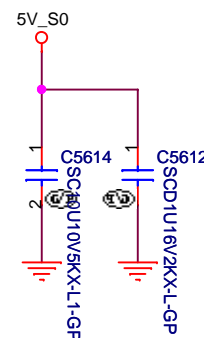
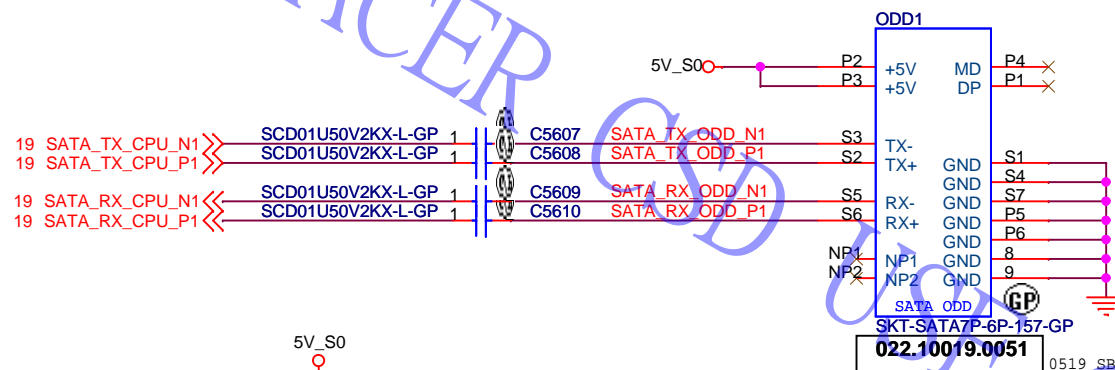
SSID = SATA

# SATA HDD Connector



AC coupling caps near connector < 100 mils

## ODD Connector



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Title			
<b>HDD / ODD / NGFF SSD</b>			
Size A4	Document Number <b>EA53-BM</b>		Rev <b>-1</b>
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AC coupling caps near connector < 100 mils



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Size  
A4

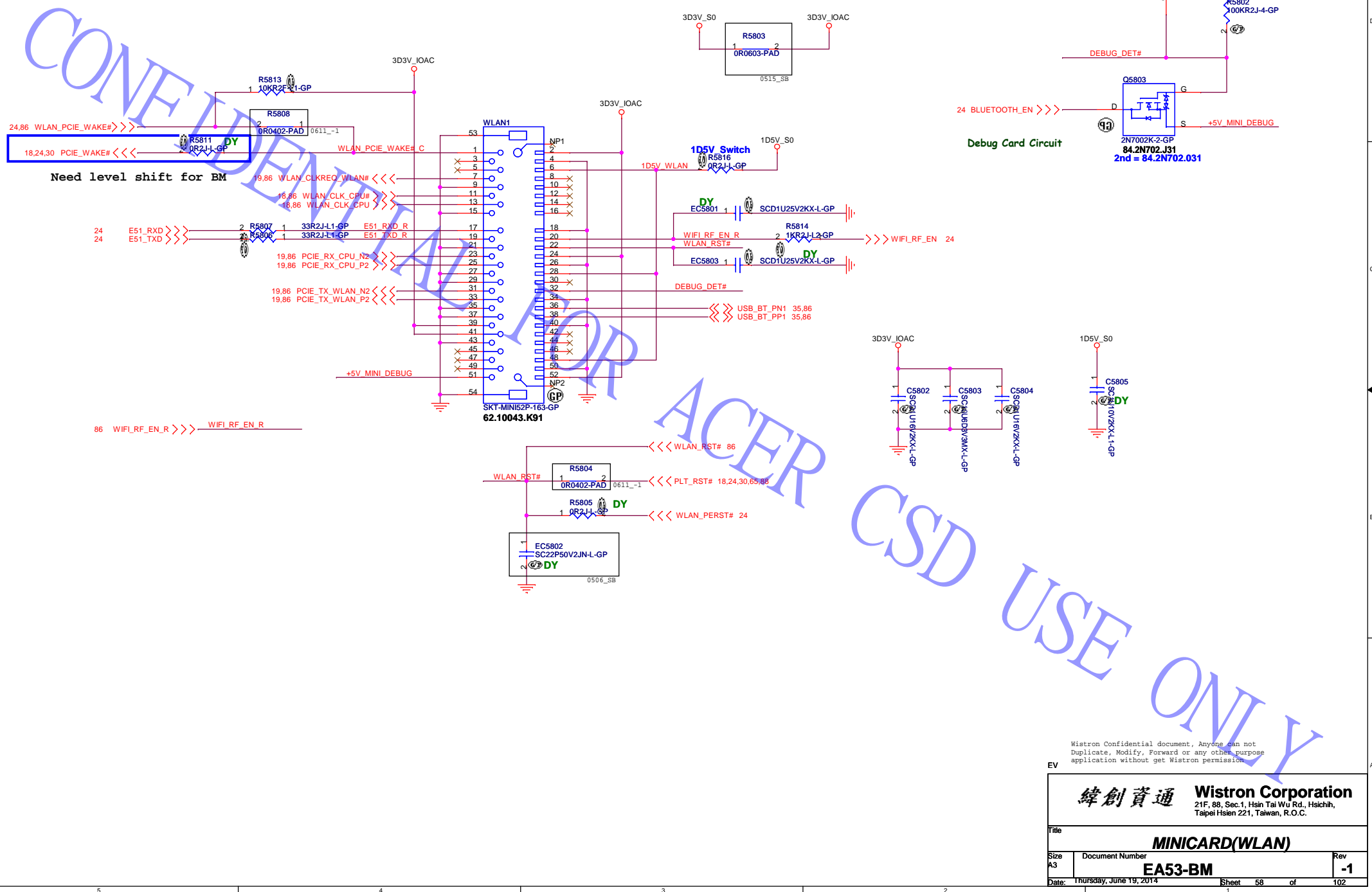
Document Number

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SSID = 3G

Mini Card Connector(WWAN)

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Title

**WWAN CONN**

Size  
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SSID = mSATA

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Mini Card Connector(mSATA)

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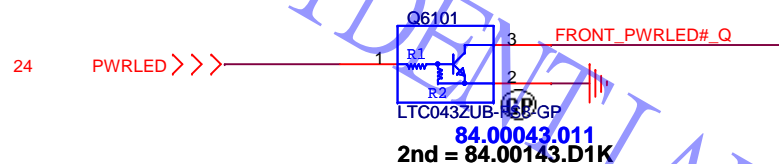
Date: Wednesday, June 04, 2014

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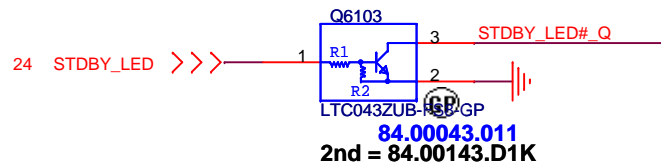
SSID = User.Interface

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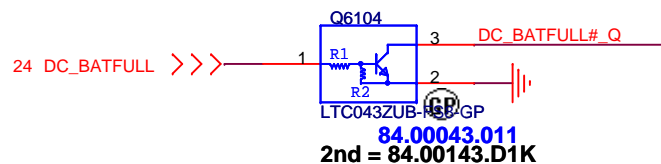
## Power button LED



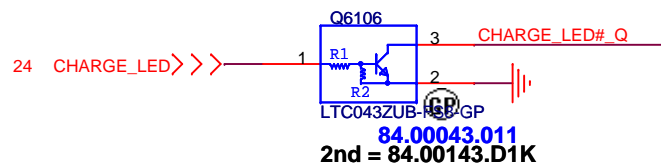
## Power STDBY\_LED



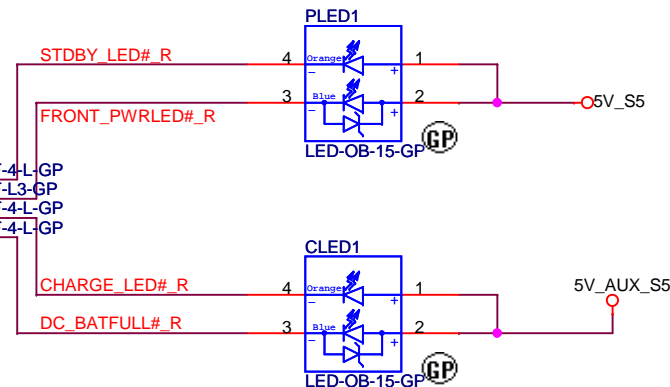
## Battery LED2 (DC\_BATFULL)



## Battery LED1 (CHARGE)



STDBY\_LED#\_Q 1 R6101 150R2F-4-L-GP  
FRONT\_PWRLED#\_Q 1 R6102 100R2F-L3-GP  
CHARGE\_LED#\_Q 1 R6103 150R2F-4-L-GP  
DC\_BATFULL#\_Q 1 R6104 150R2F-4-L-GP



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**LED Bard/Power Button**

Size  
A4

Document Number

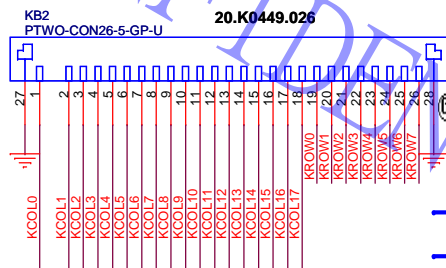
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KB2 20.K0449.026

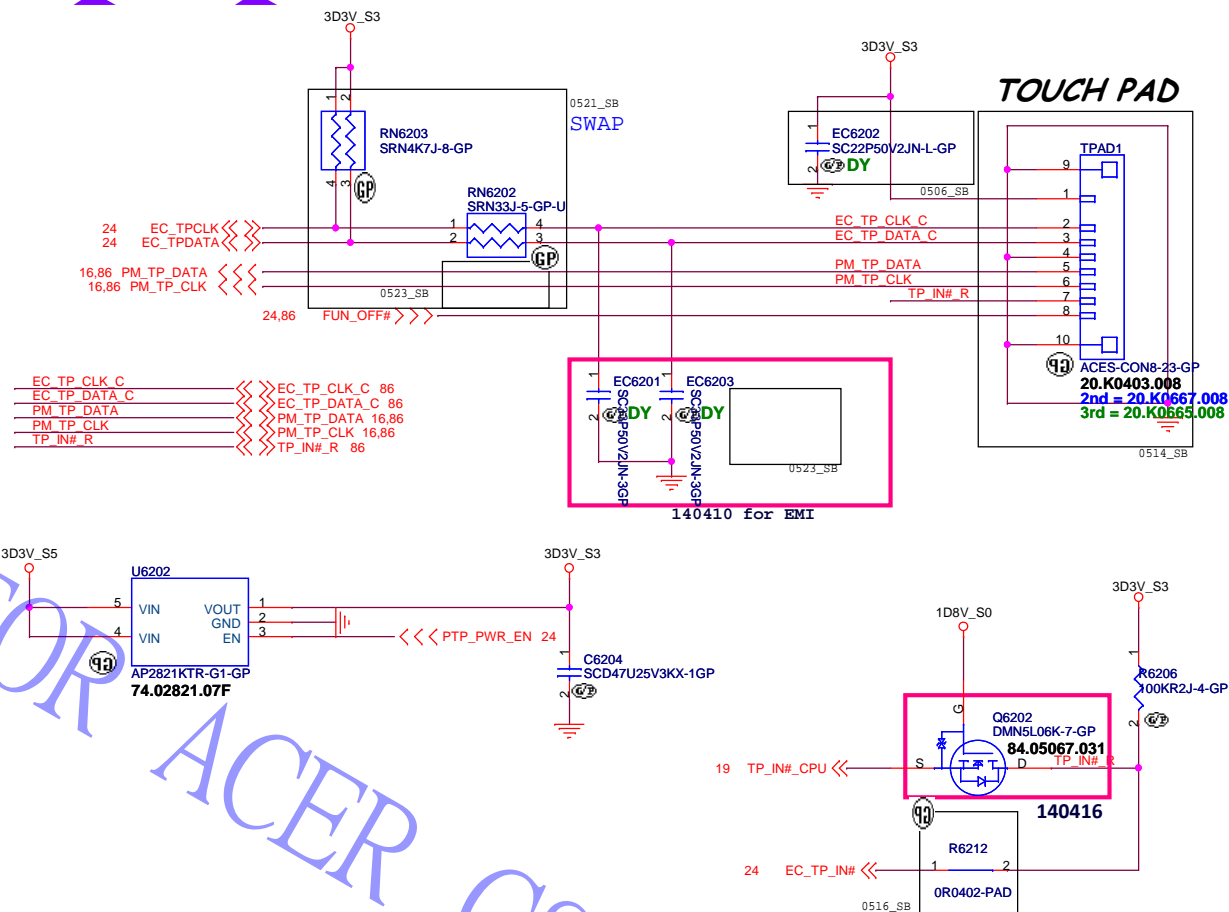


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KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

```

26 K/B 1



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### Key Board/Touch Pad

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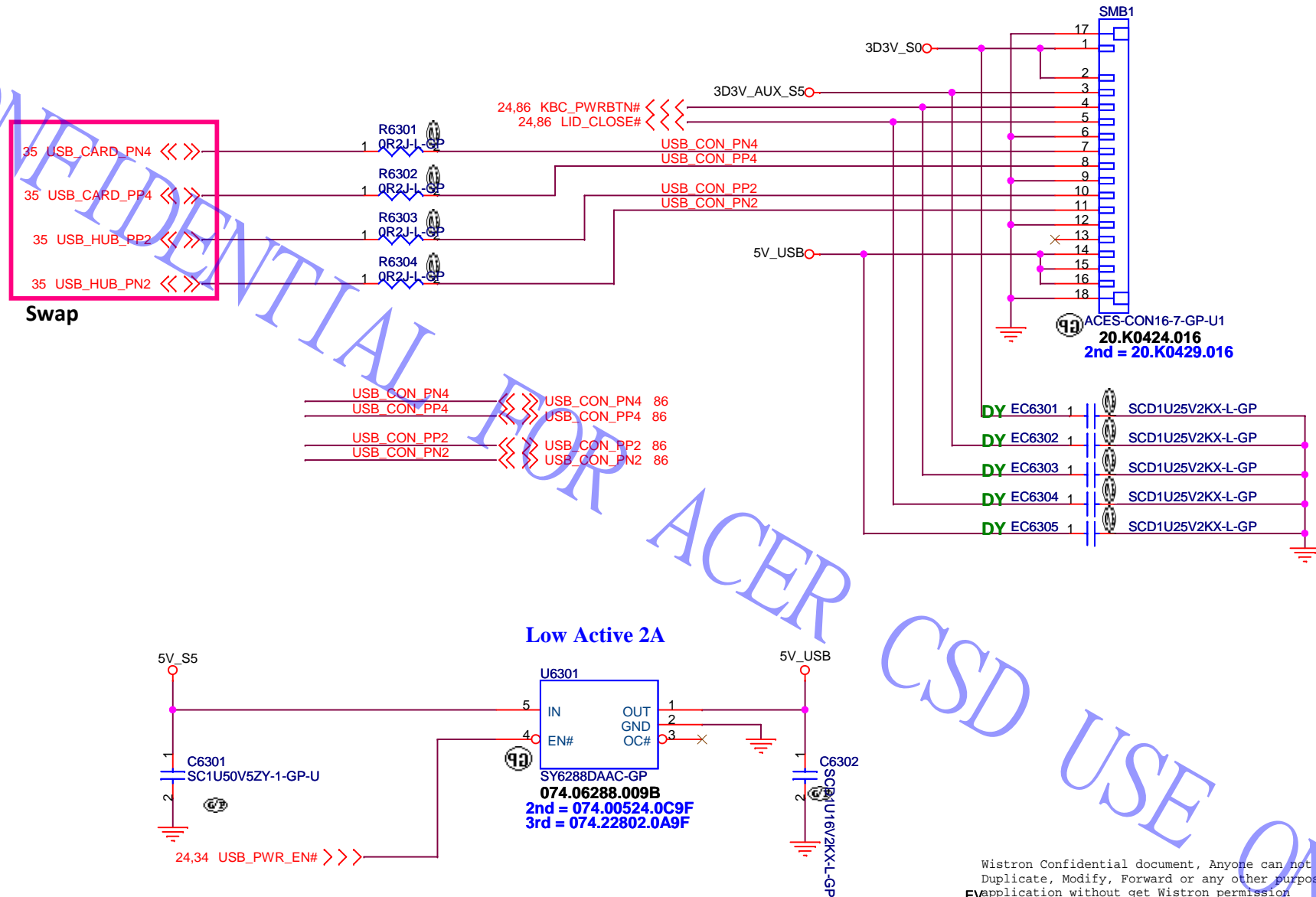
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**IO Board Connector**

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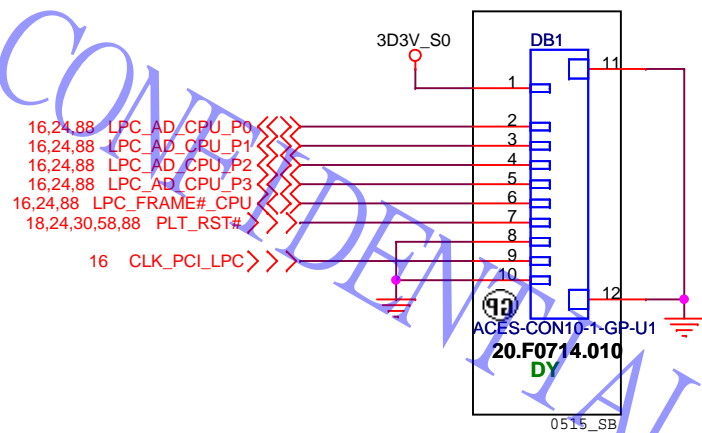
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Size <div>A4</div>	Document Number <div>EA53-BM</div>	Rev <div>-1</div>
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## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"  
\*SDO="L"; address="38h"

\*CS="H"; mode="I2C"  
CS="L"; mode="SPI"

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G Sensor			
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Title

**Thunderbolt (1/5)**

Size  
A4

Document Number

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Rev  
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Title

**Thunderbolt (2/5)**

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**Thunderbolt (3/5)**

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Title

**Thunderbolt (4/5)**

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GPU(PEG)

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GPU (DIGITALOUT)			
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Rev	EA53-BM	Rev	-1
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Title			
GPU-VRAM1,2 (1/4)			
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Title			
GPU-VRAM3,4 (2/4)			
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Title

GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)					
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Title RT8812A VGA CORE	
Size Custom	Document Number EA53-BM
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3D3V\_S0 to 3D3V\_VGA\_S0  
1D05V\_VTT to 1D05V\_VGA\_S0  
EA40-HW 1

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DISCRETE VGA POWER	
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Title		
Switchable GFX LCD(1/2)		
Size	Document Number	Rev
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Title

**Switchable GFX LCD(2/2)**

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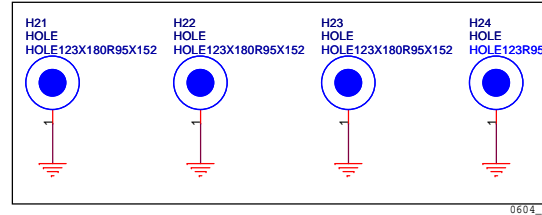
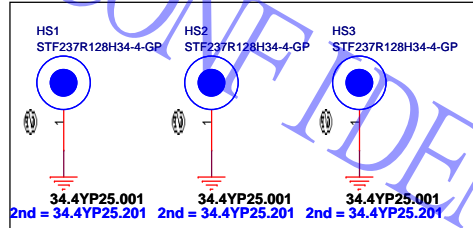
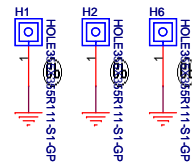
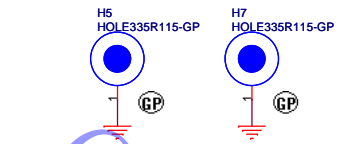
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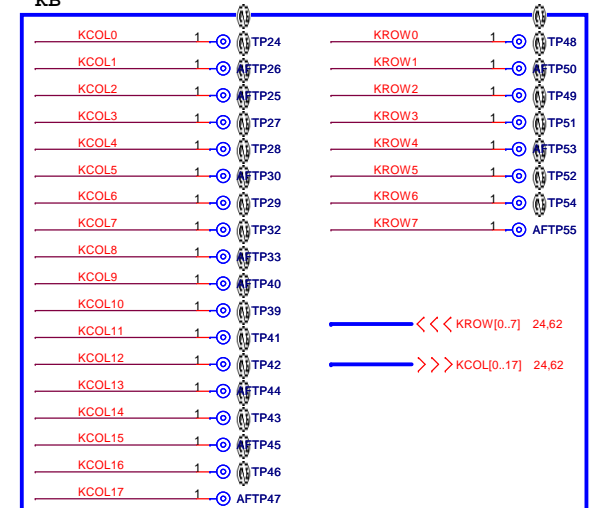
Date: Wednesday, June 04, 2014

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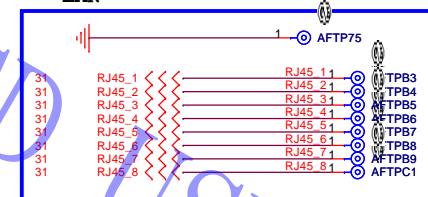
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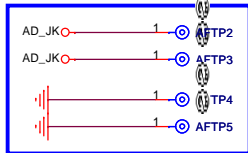
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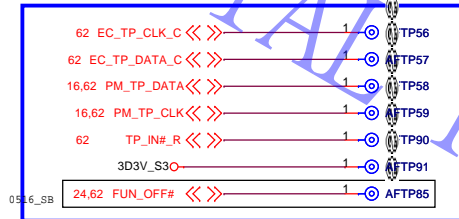
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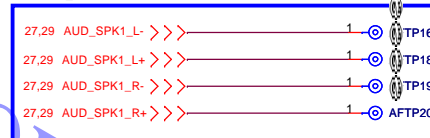
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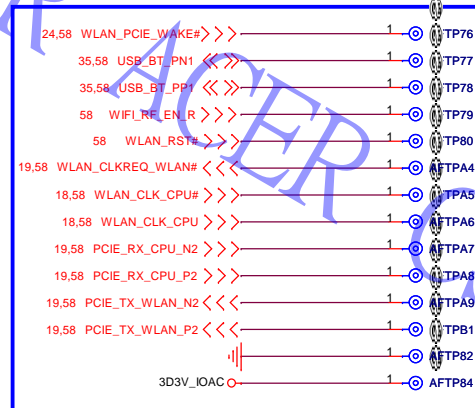
## Touch PAD



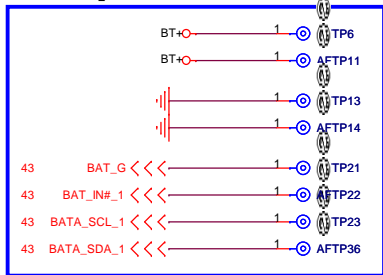
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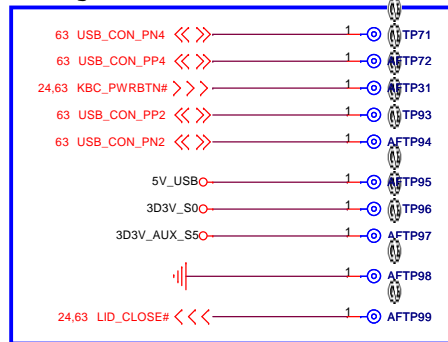
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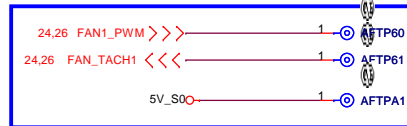
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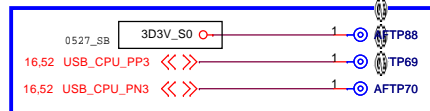
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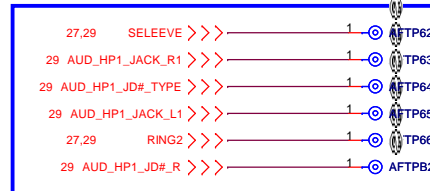
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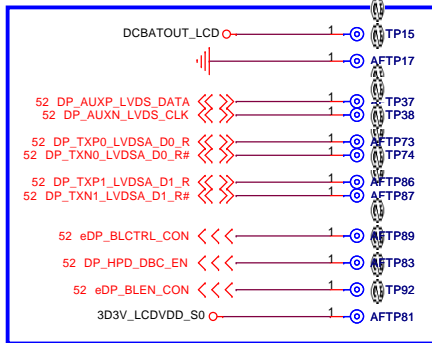
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## LOUT



## EDP



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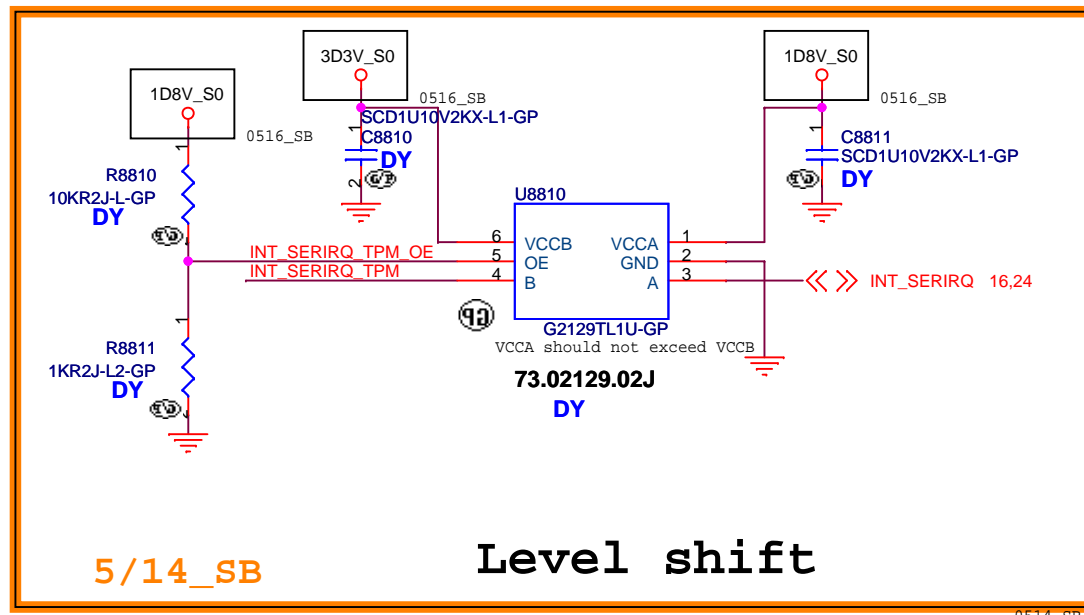
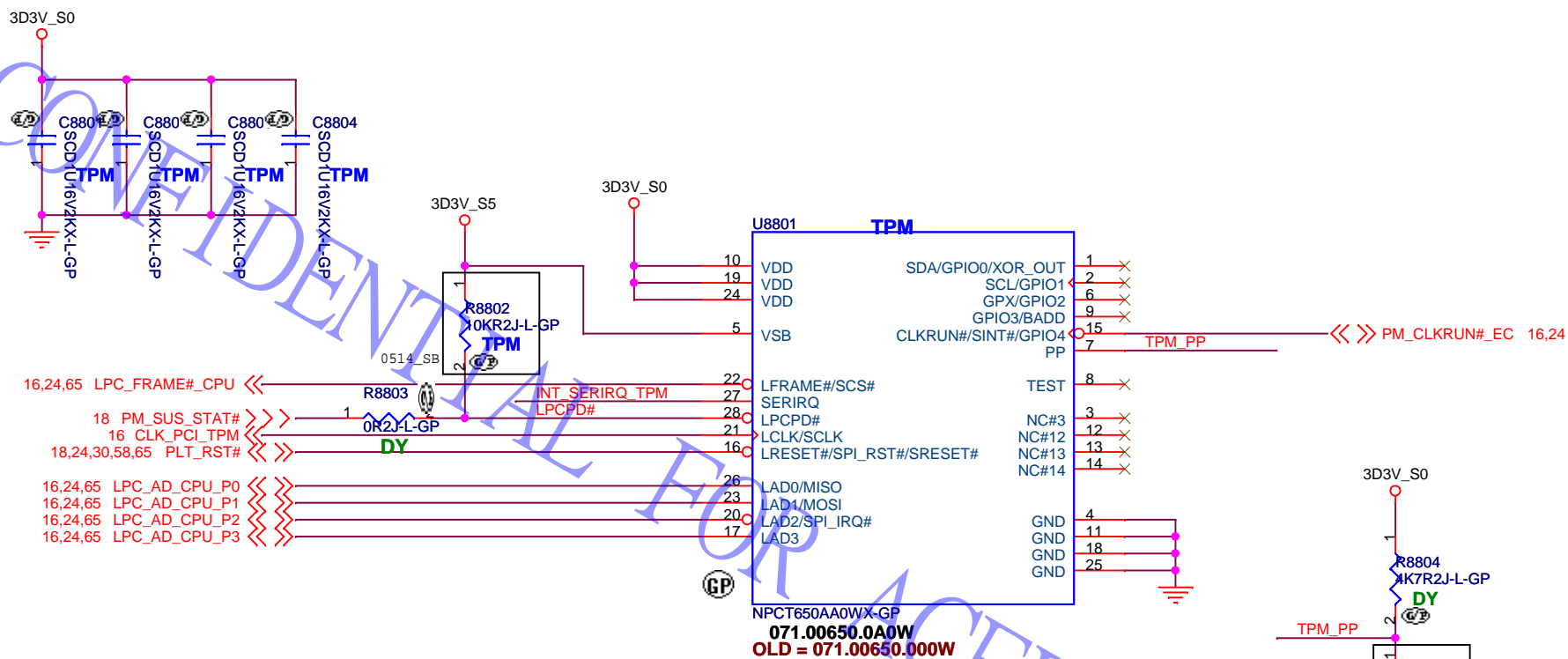
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SSID = Finger Print

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SSID = Smart Card

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SSID = Docking

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SSID = Intel LAN

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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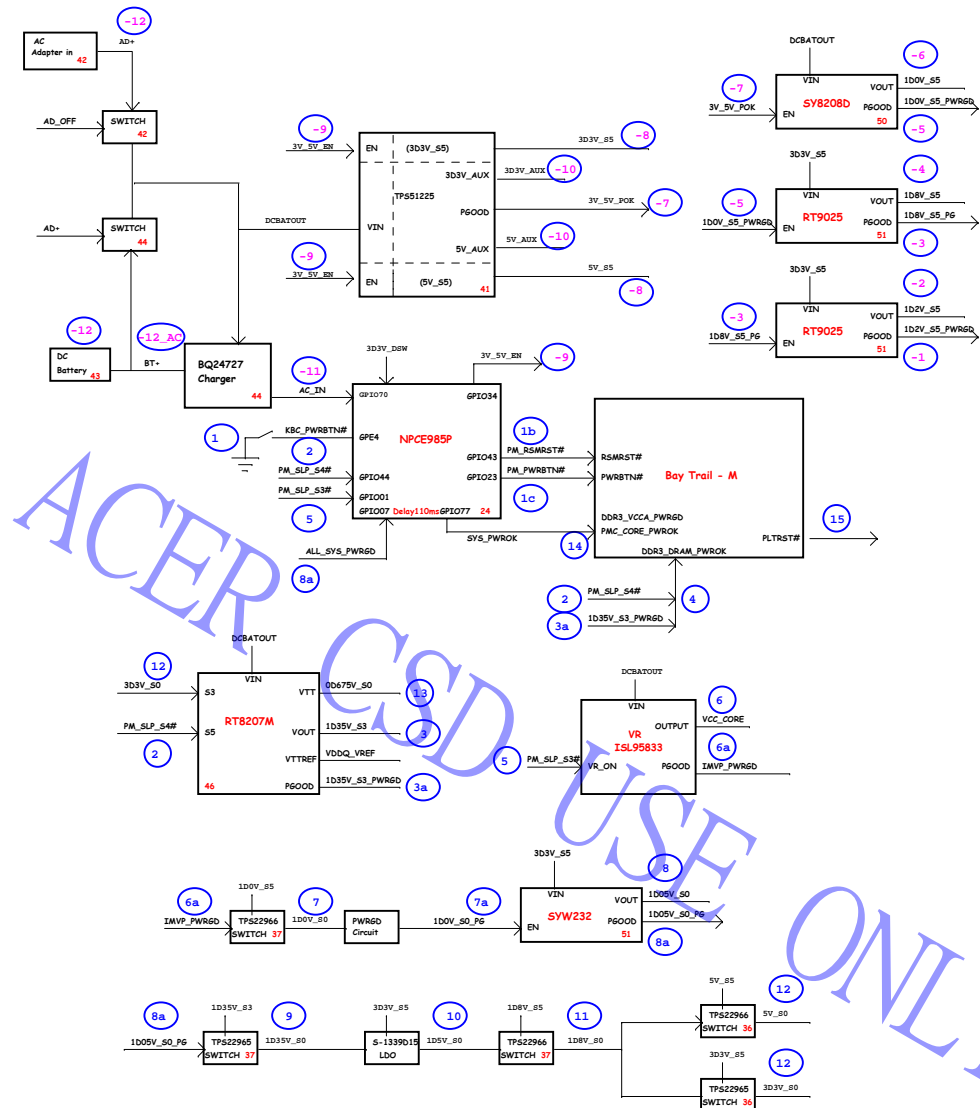
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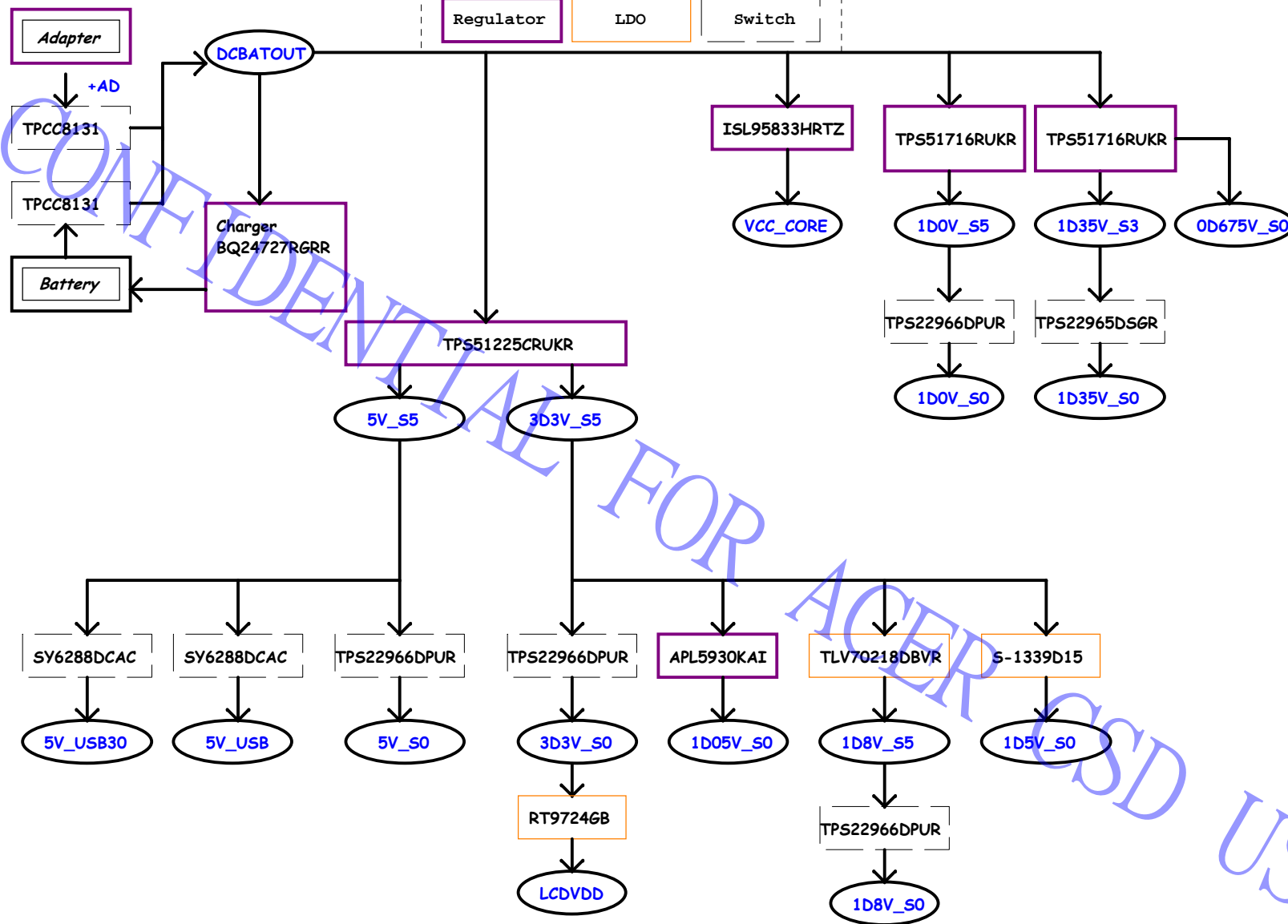
Timing diagram for the 3.3V Level showing the sequence of signals during a reset event. The signals include:

- RTC\_AUX\_S5
- RTC\_RST#
- 3D3V\_AUX/SV\_AUX
- ECRST#
- 3V\_SV\_EN
- 5V\_S5/3D3V\_S5
- 1D0V\_S5
- 1D0V\_S5\_PWRGD
- 1D8V\_S5
- 1D8V\_S5\_P6
- 1D2V\_S5
- 1D2V\_S5\_PWRGD
- RSMRST#\_KBC
- PM\_SLP\_S4#
- DDR3\_DRAM\_PWROK
- 1D35V\_S3
- PM\_SLP\_S3#
- VCC\_CORE & GFX\_CORE
- IMVP\_PWRGD
- 1D0V\_S0
- 1D0V\_S0\_P6
- 1D05V\_S0
- 1D05V\_S0\_P6 (ALL\_SYS\_PWRGD to EC)
- 1D35V\_S0 & 1D35V\_CRT\_S0
- 1D5V\_S0
- 1D8V\_S0
- 3D3V\_S0 & 5V\_S0
- 0D675V\_S0
- SYS\_PWROK (Base on ALL\_SYS\_PWRGD to delay 110ms)
- COREPWROK
- 1.35V Level
- DDR3\_VCCA\_PWRGD
- FLT\_RST#

Key timing points:

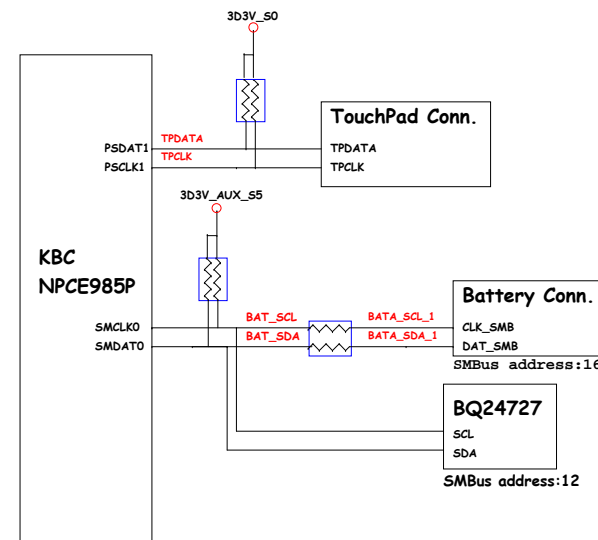
- $T_1 = 10 \mu s$
- $T_1 = 110ms$



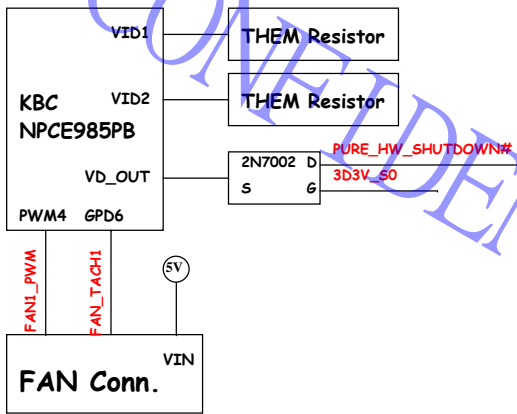


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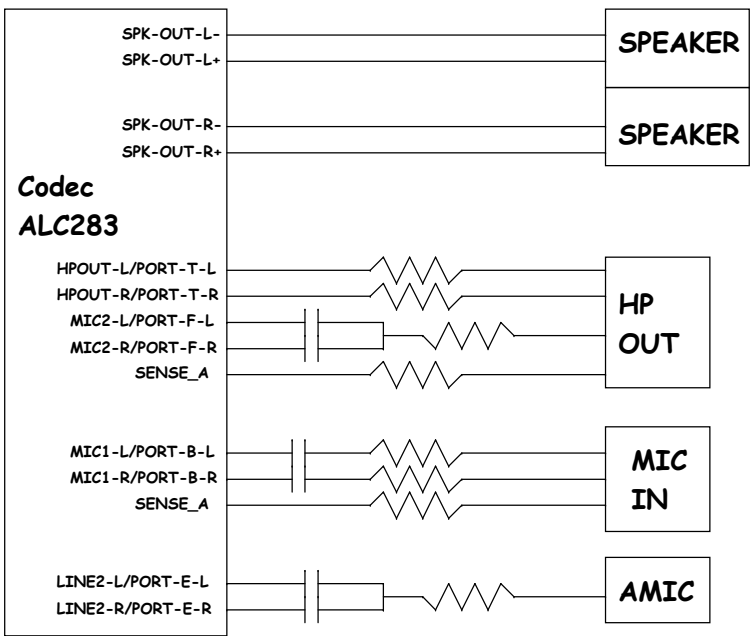
### *k3c' SMBus Block Diagram*



Thermal Block Diagram



Audio Block Diagram



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